CHAPTER 5
SOLID-STATE TRANSMITTERS

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5.1 INTRODUCTION

Solid-state devices have largely superseded vacuum tubes in logic and other low-power circuits and even in some very high power applications such as power supplies and power converters below 1 MHz. The only exception seems to be cathode-ray tubes (CRTs), which are less costly than large plasma displays. In radar transmitters, the transition from high-power klystrons, traveling-wave tubes (TWTs), crossed-field amplifiers (CFAs), and magnetrons to solid-state has been more gradual because the power output of individual solid-state devices is quite limited. However, compared with tubes, solid-state devices offer many advantages:

1. No hot cathodes are required; therefore, there is no warmup delay, no wasted heater power, and virtually no limit on operating life.

2. Device operation occurs at much lower voltages; therefore, power supply voltages are on the order of volts rather than kilovolts. This avoids the need for large spacings, oil filling, or encapsulation, thus saving size and weight and leading to higher reliability of the power supplies as well as of the microwave power amplifiers themselves.

3. Transmitters designed with solid-state devices exhibit improved mean time between failures (MTBF) in comparison with tube-type transmitters. Module MTBFs greater than 100,000 h have been measured.

4. No pulse modulator is required. Solid-state microwave devices for radar generally operate Class-C, which is *self-pulsing* as the RF drive is turned on and off.

5. Graceful degradation of system performance occurs when modules fail. This results because a large number of solid-state devices must be combined to provide the power for a radar transmitter, and they are easily combined in ways that degrade gracefully when individual units fail. Overall power output, in decibels, degrades only as 20 log r, where r is the ratio of operating to total amplifiers.

6. Extremely wide bandwidth can be realized. While high-power microwave radar tubes can achieve 10 to 20 percent bandwidth, solid-state transmitter modules can achieve up to 50 percent bandwidth or more with good efficiency.

7. Flexibility can be realized for phased array applications. For phased array

systems, an active transceiver module can be associated with every antenna element. RF distribution losses that normally occur in a tube-powered system between a point-source tube amplifier and the face of the array are thus eliminated. In addition, phase shifting for beam steering can be implemented at low power levels on the input feed side of an active array module; this avoids the high-power losses of the phase shifters at the radiating elements and raises overall efficiency. Also, peak RF power levels at any point are relatively low since the outputs are combined only in space. Furthermore, amplitude tapering can be accomplished by turning off or attenuating individual active array amplifiers.

The general replacement of high-power microwave tubes by solid-state devices has proceeded more slowly than was once forecast. With hindsight, the reason for this is that it is usually too costly to use solid-state devices to replace a pulsed RF tube directly while operating at the same peak power and duty cycle. This is true because microwave semiconductor devices have much shorter thermal time constants than RF tubes (milliseconds rather than seconds). The result is that a microwave transistor that is capable of perhaps 50-W average power cannot handle much more than 100 to 200 W of peak power without overheating during the pulse. The short pulse lengths and low duty cycles typical of older tube-type radars would thus make very inefficient use of the average power capabilities of microwave transistors. For example, to replace the old, well-proven 5J26 L-band magnetron that develops 500 W of average RF power at 0.1 percent (typical) duty cycle would require 2500 to 5000 of the 50-W transistors just mentioned. In other words, microwave transistors are much more cost-effective when the required radar system average power can be provided by a lower peak power at a higher duty cycle. As a result, there have been relatively few direct replacements of older low-duty-cycle transmitters by solid-state transmitters; the AN/SPS-40 is an interesting exception to this rule and will be discussed later. For new radar systems, the system designers have been motivated by these considerations to choose as high a duty cycle as possible, both to reduce the peak power required and to permit using solid-state devices at a reasonable cost. With a 10 percent duty cycle, for example, the 500-W average power mentioned earlier in the paragraph could be provided by only 25 to 50 of the 50-W transistors.

The decision to use a high transmitter duty cycle, however, has significant impact on the rest of the radar system. Operation at a high duty cycle generally requires the use of pulse compression to provide the desired unambiguous range coverage together with reasonably small range resolution. Other consequences follow in turn: the wide transmitted pulse used with pulse compression blinds the radar at short ranges, so a "fill-in" pulse must also be transmitted and processed. To prevent points of strong clutter from masking small moving targets, the signal processor must achieve low pulse compression time sidelobes and high clutter cancellation ratio. As a result, it is much easier to design a solid-state transmitter as part of a new system than it is to retrofit one into an old system that usually does not have all these features.

High-power microwave transistors have been developed more quickly at HF through L band than at higher-frequency bands, so the widest use of solid-state transmitters has been at these lower bands, as shown in Table 5.1. Note, also, that solid-state transmitters at UHF and below have generally been much higher in peak and average power than those at L band.

The use of solid-state does not eliminate all the problems of transmitter design, of course. The RF combining networks must be designed with great care and skill to minimize combining losses in order to keep transmitter efficiency

TABLE 5.1 Fielded Solid-State Transmitters

System	Contractor	Frequency, MHz	Peak power, kW	Duty cycle	Average power, kW	No. of modules	Peak power per module, W	Year fielded
ROTHR	Raytheon	5–30	210	CW	210	84	3000	1986
NAVSPASUR*	Raytheon	218	850	CW	850	2666	320	1986
SPS-40*	Westinghouse	400–450	250	1.6%	4	112	2500	1983
PAVE PAWS†	Raytheon	420–450	600	25.0%	150	1792	340	1978
BMEWS*	Raytheon	420–450	850	30.0%	255	2500	340	1986
TPS-59	GE	1200–1400	54	18.0%	9.7	1080	50	1975
TPS-59‡	GE	1200–1400	54	18.0%	9.7	540	100	1982
SEEK IGLOO	GE	1200–1400	29	18.0%	5.2	292	100	1980
MARTELLO*	Marconi	1250–1350	132	3.75%	5	40	3300	1985
RAMP	Raytheon	1250–1350	28	6.8%	1.9	14	2000	1986
SOWRBALL	Westinghouse	1250–1350	30	4.0%	1.2	72	700	1987

*Solid-state replacements of tube-type transmitters.
†Parameters per array face.
‡Upgraded with 100-W peak power modules.

high. Suitable isolation from excessive voltage–standing-wave ratio (VSWR) must be provided to protect the microwave transistors, and their harmonic power output must be properly filtered to meet MIL-STD-469 and other specifications on RF spectrum quality. Because most microwave transistors operate Class-C, no pulse modulators are required, but Class-C operation makes it more difficult to provide controlled shaping of the RF rise and fall time for spectrum control. Also, just as in tube-type transmitters, energy management is still crucial. Each dc power supply must have a capacitor bank large enough to supply the energy drawn by its solid-state modules during an entire pulse, and each power supply must recharge its capacitor bank smoothly between pulses without drawing an excessive current surge from the power line. While the required power supply is generally not a "catalog" power supply, there are plenty of solid-state devices and circuits available to satisfy these requirements.

As a result of unavoidable losses in combining the outputs of many solid-state devices, it is especially tempting to avoid combining before radiating, since combining in space is essentially lossless. For this reason, many solid-state transmitters consist of modules that feed either rows, columns, or single elements of an array antenna. Especially in the last-named case, it is necessary to build the modules (and probably their power supplies) into the array structure. Furthermore, locating the modules at the antenna avoids the losses of long waveguide runs. Nevertheless, there are cases where building that much equipment weight into the antenna is undesirable, which may force designers to stay with conventional combining schemes. One such case is shipboard radars; the antenna is always mounted as high on the ship as possible, where weight must be minimized to maintain roll stability, and where access for maintenance is extremely difficult.[1]

Because of the large number of individual modules in a typical solid-state transmitter, failure of an individual or a few modules has little effect on overall transmitter performance. However, the module outputs add as voltage vectors,

so that loss of 2 of 10 modules (or 20 percent of 1000 modules) results in a reduction to 80 percent of voltage output, which is 64 percent of power output; but even this is only a 2-dB reduction (the difference between 64 and 80 percent of the power ends up in the combiner loads or in sidelobes if the combining is in space). As a result of this "graceful degradation," overall reliability of solid-state transmitters is very high even if maintenance is delayed until convenient scheduled periods; however, this advantage should not be abused. Consider a case where 20 percent of 1000 modules are allowed to fail before output power falls below requirements, and assume that maintenance occurs at scheduled 3-month intervals. In this case, module MTBF need only be 22,000 h to provide 90 percent confidence that the transmitter will not "fail" in less than 3 months; but the cost of replacement modules and labor would be very unattractive, since nearly 40 percent of the transmitter would have to be replaced every year. Higher MTBFs are thus essential to ensure that the transmitter is not only available but also affordable. Fortunately, solid-state module reliability has proved to be even better than the MIL-HDBK-217 predictions; AN/FPS-115 (PAVE PAWS), for example, actual transceiver module MTBF, including the receiver transmit/receiver (T/R) switches and phase shifters as well as the power amplifiers, has grown to 141,000 h, which is 2.3 times the predicted value. In fact, MTBF for the output power transistors measures better than 1.1 million h.[2]

5.2 SOLID-STATE MICROWAVE POWER GENERATION

Although the RF power-generating capability of single solid-state devices is small with respect to the overall peak and average power requirements of a radar transmitter, solid-state devices can be used quite effectively. Large peak and average powers can be attained by combining the outputs of hundreds or thousands of identical solid-state amplifiers. The power output level from a particular device is a function of the exact operating frequency and the operating conditions, namely, the pulse width and duty cycle, and within normal operating constraints bipolar transistors can provide power outputs in the 50-W through 500-W range. These devices have been used for successful designs in the UHF through L-band frequency ranges, as noted in Table 5.1. Bipolar devices satisfy system requirements of reliability, electrical performance, packaging, cooling, availability, and maintainability. In fact, these devices offer an attractive alternative to tube operation at the lower frequencies.

At higher frequencies, and especially for microwave phased array applications where a physically small module with transmit and receive functions is necessary, the gallium arsenide field-effect transistor (GaAs FET) and its associated batch-processed monolithic microwave integrated circuitry (MMIC) can be used. GaAs FETs are well established as low-noise devices up to 60 GHz;[3] and, with individual cell-combining techniques,[4] GaAs FETs can be used as power amplifiers in the 1- to 20-GHz range. In general, the attribute that makes GaAs an attractive technology is that the GaAs FET can be fully integrated with the passive circuitry that is necessary to provide the biasing, loading, filtering, and switching functions that are necessary for multistage transceiver module designs. As a result of fundamental device limitations, however, this approach is not envisioned

as a cost-effective alternative for module designs that require power outputs exceeding 25 to 30 W.

For the upper end of the solid-state microwave spectrum, i.e., the millimeter-wave range, the single-port microwave diode can be used as a low-power oscillator. Unfortunately, the power output and efficiency of these devices are in general very low; in fact, the efficiency is significantly lower than that of their tube counterparts. However, CW and pulsed power output are attainable up to 300 GHz. Gunn and IMPATT diodes are the devices that offer the most promise for millimeter-wave solid-state operation.

Brief descriptions of these device types and their associated technologies are given in the following subsections.

Microwave Bipolar Power Transistors. The silicon bipolar power transistor is a common device choice for a solid-state system. At the lower frequencies, especially below 3 GHz, this component provides adequate performance at the lowest cost among competing solid-state technologies. Amplifier design is realizable for frequencies up through S Band, where the tradeoff between device performance and overall system cost begins to reach a point of diminishing returns. The silicon bipolar transistor technology is very mature, and, with the continuing advances in device processing, packaging, and circuit design techniques, manufacturers should be able to continue demonstrating increased levels of power output, bandwidth, and reliability for these transistors. In addition, as a relative figure of merit, the cost per watt of device output power has been decreasing as a result of improvements in processing yields and as a result of increased automated or semiautomated assembly techniques.

Microwave power transistors can be considered complex hybrid circuits and are generally single-chip or multichip devices. For devices with very high power output, several transistor dice are always combined in parallel within a small hermetic ceramic package. In addition, some form of internal impedance prematching circuitry is often included in order to preserve the high intrinsic bandwidth of the semiconductor chip and to make the task of external impedance matching easier. The internal matching also increases the terminal impedances of the packaged device to a level where the component losses of the circuitry external to the transistor become less critical.

The processing and planar layout of these chips is somewhat standardized among manufacturers. Figure 5.1 shows a partial cross section of a typical microwave bipolar power transistor chip. The structure is an NPN silicon device with a vertical diffusion profile; i.e., the collector contact forms the bottom layer of the chip. The P-type base region has been diffused or implanted into the collector, the N-type emitter has been diffused or implanted into the base, and both base and emitter regions are accessible from the top surface of the chip. The collector region consists of an N-doped, low-resistivity epitaxial layer that is grown on a very low resistivity silicon substrate. The characteristics of the epitaxial layer, i.e., thickness and resistivity, can determine the upper limit of performance of the device in terms of ruggedness, efficiency, and saturated power output.

The fundamental limitation on high-frequency transistor performance is the overall collector-to-emitter delay time. If a signal is introduced to either the base or the emitter, four separate regions of attenuation or time delay are encountered: the emitter-base junction capacity charging time, the base transit time, the col-

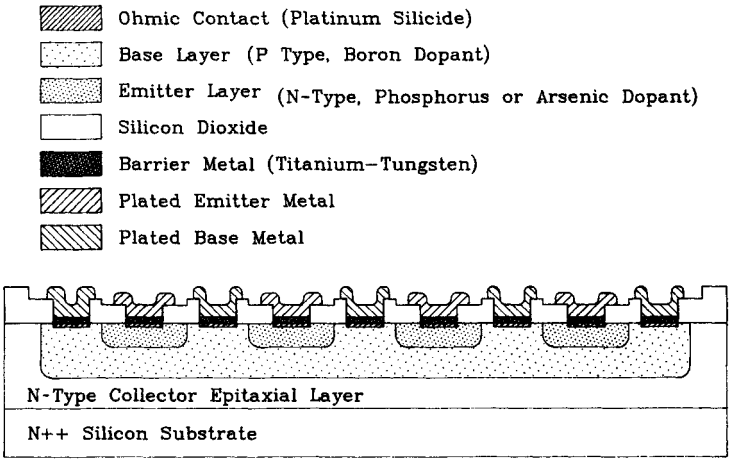

FIG. 5.1 Cross section of a microwave bipolar transistor chip. (*Reprinted with permission from E. D. Ostroff et al., "Solid-State Transmitters," Artech House, Norwood, Mass., 1985.*)

lector depletion-layer transit time, and the collector capacitance-resistance charging time. High-frequency transistor design is concerned with optimizing the physical parameters that contribute to the time-delay components.[5]

For high-power chips, the design challenge is to maintain a uniform high current density over a large emitter area with a minimum temperature rise. High-frequency devices require shallow, narrow, high-resistance base regions under the emitter region. This causes most of the current carried in the device to be crowded along the periphery of the emitter. Thus, in order to maximize the current-handling capability of the device and hence the power output capability of the device, the emitter periphery is maximized. Since the capacitance of the collector-base junction appears as a deleterious parasitic electrical component, the emitter-periphery to base-area ratio, or *Ep/Ba*, is maximized where possible. Generally, higher-frequency devices exhibit higher *Ep/Ba* ratios; and to obtain a high *Ep/Ba* ratio very fine line geometries are required, where the term *geometry* refers to the surface construction details of the transistor.

One limit on the RF power output capability of the transistor is the breakdown voltage of the collector-base junction. Within that limit, the maximum practical level of power output that can be obtained from a single transistor over a given bandwidth is governed by two further limitations: the thermal-dissipation limit of the device and the terminal input or output impedance limit of the device. These latter two limitations are somewhat related by virtue of the physical construction of typical devices.

Active transistor area on the surface of the chip is divided into cells, where the cell size is most often custom-designed for a particular application or range of applications. Pulse width and duty cycle or, as a result, the peak and average dissipated power are the parameters that determine the cell size and arrangement of cells on a chip. As devices become larger and the dissipative heat flux from the top surface of the die to the bottom layer of the transistor increases, the junction temperature increases to the point where the transistor becomes thermally limited.

The ultimate operating junction temperature of the transistor is largely dependent on the transient heating that will be encountered and the layout and area of the individual cells. For devices that are designed to operate for long pulses or CW, an increase in the average power capability of the transistor can be achieved by dividing the active area of a transistor into small, thermally isolated cell areas.

There is a thermal time constant associated with the numerous thermally resistive layers between the transistor junction and the heat sink or cold plate to which the device is attached. This occurs because each layer (silicon, ceramic, transistor flange) not only has a thermal resistance but also exhibits a thermal capacity. Since the overall thermal time constant for a typical L-band power transistor may be on the order of hundreds of microseconds, the tradeoff between peak and average power versus device size can be significant for typical radar pulse widths in the 20- to 1000-μs range. Devices that operate for short-pulse and low-duty-cycle applications, such as DME (distance-measuring equipment), Tacan, and IFF (identification, friend or foe) systems, differ in design from the devices that have been designed for the longer pulse widths and moderate-duty-cycle waveforms that are more typical for surveillance radars. Very high duty cycles or CW operation dictates careful thermal design. An illustration of the thermal-time-constant effect, as it relates to a train of RF pulses, is shown in Fig. 5.2. Table 5.2 illustrates some reported device applications and their general performance characteristics. A photograph of the 115-W UHF transistor used for the PAVE PAWS transmitter is shown in Fig. 5.3, and the schematic, shown in Figure 5.4, may be considered typical for a packaged multichip 100-W L-band transistor.

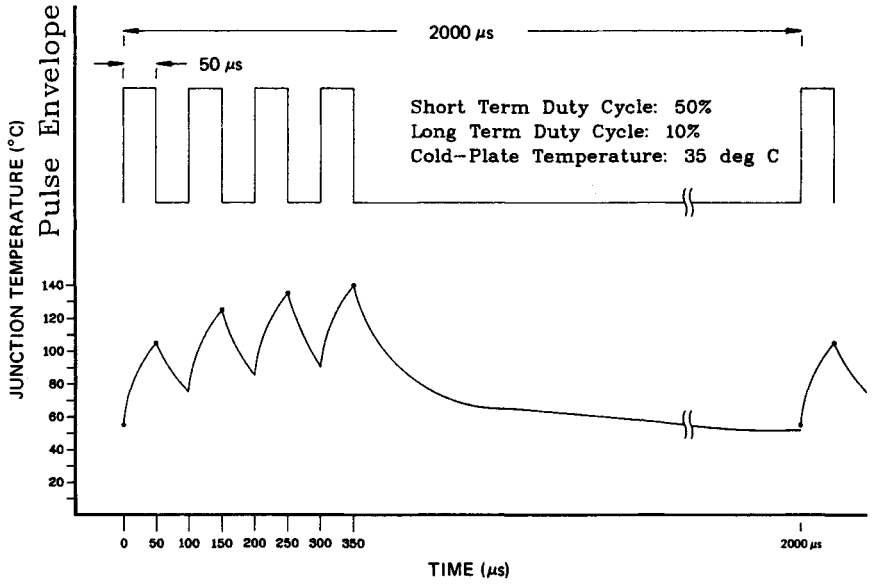

FIG. 5.2 Transient thermal response of a Class-C-biased silicon power transistor for a pulsed RF input.

TABLE 5.2 System Applications for Microwave Power Transistors*

System	Frequency, MHz	Pulse/duty	Transistor performance		
			Peak power, W	Gain, dB	Efficiency, percent
OTH	5–30	CW	130	14.0	60
NAVSPASUR	217	CW	100	9.2	72
AN/SPS-40	400–450	60 μs at 2%	450	8.0	60
PAVE PAWS	420–450	16 ms at 20%	115	8.5	65
BMEWS	420–450	16 ms at 20%	115	8.5	65
AN/TPS-59	1215–1400	2 ms at 20%	55	6.6	52
RAMP	1250–1350	100 μs at 10%	105	7.5	55
MARTELLO S723	1235–1365	150 μs at 4%	275	6.3	40
MATCALS	2700–2900	100 μs at 10%	63	6.5	40
AN/SPS-48	2900–3100	40 μs at 4%	55	5.9	32
AN/TPQ-37	3100–3500	100 μs at 25%	30	5.0	30
HADR	3100–3500	800 μs at 23%	50	5.3	35

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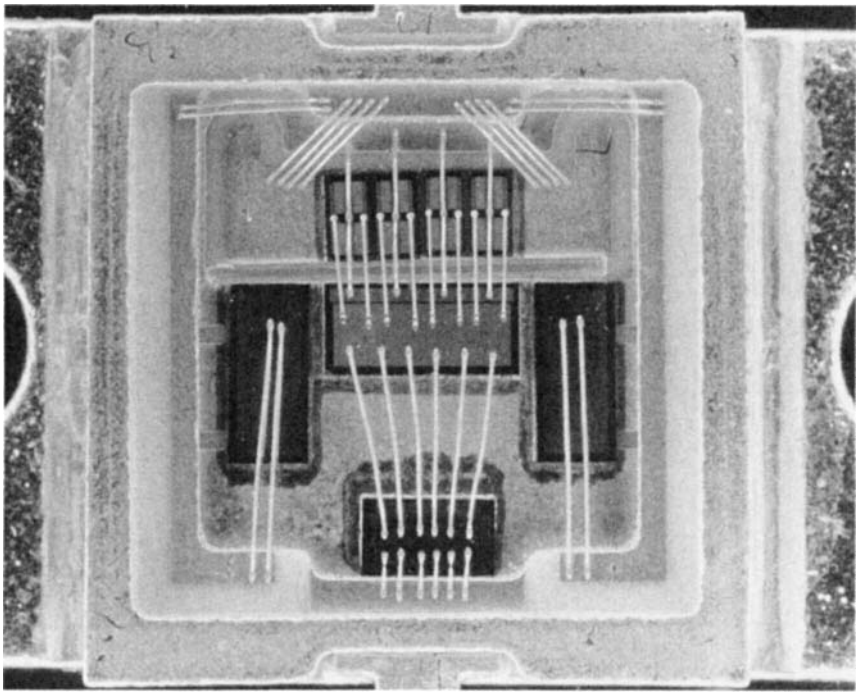


FIG. 5.3 A UHF 115-W power transistor for long pulse and high duty cycle, used in the PAVE PAWS transmitter. (*Photograph courtesy of M/A-COM, PHI.*)

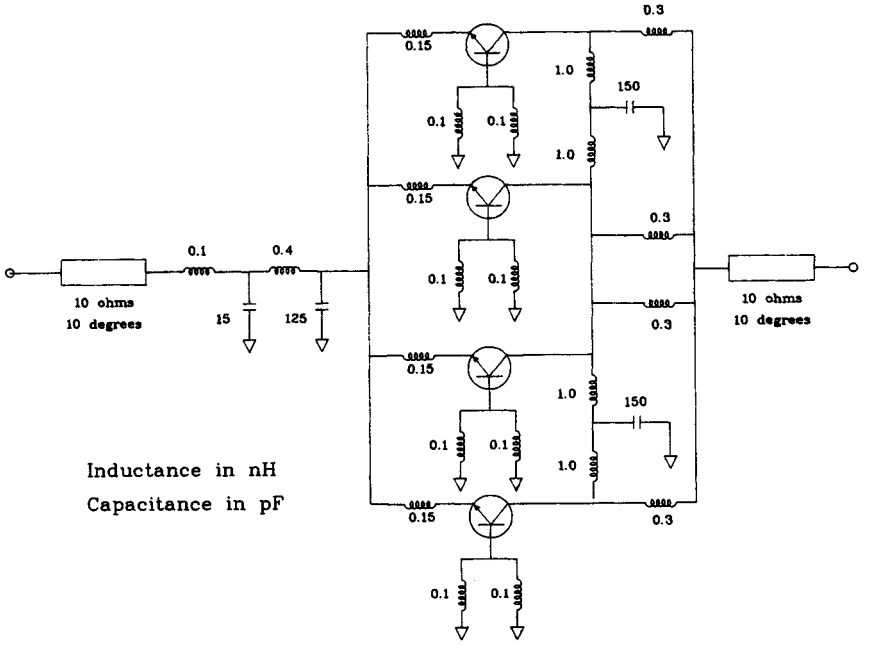


FIG. 5.4 Circuit schematic of an internally input- and output-matched 100-W L-band power transistor.

Microwave Field-Effect Transistors (FETs). Silicon power FETs have demonstrated power output characteristics comparable to the silicon bipolar transistor in the 0.1- to 1.0-GHz frequency range[6]; however, power FETs that are made from gallium arsenide (GaAs) are limited in power output capability, primarily because of the poor thermal conductivity of GaAs and lower typical breakdown voltages; but they are capable of much higher frequency operation than silicon devices.[7] In addition, the GaAs FET can be utilized in a monolithic format, where the remaining passive circuitry of the amplifier is totally integrated on the same substrate with the active device.

GaAs Power FETs. In an FET, the flow of charge carriers between the source and drain electrodes is modulated by one or more gate electrodes, and when the FET is operated as a power device, it may be considered as a simple current switch. Power devices in GaAs are commonly built as metal-semiconductor field-effect transistors (MESFETs), so called because the gate metal is deposited directly onto the semiconductor channel region, forming a Schottky barrier. Power FETs that are fabricated on GaAs exhibit substantially higher frequency performance than similar devices fabricated on silicon because GaAs has a higher electron bulk mobility and a greater maximum electron drift velocity than silicon. In addition, the electron mobility in epitaxial GaAs approaches the bulk value; hence GaAs FETs exhibit lower parasitic series resistances and higher transconductances than silicon FETs with similar geometries. Electrons in GaAs travel at approximately twice the speed that is possible in sil-

icon. In addition, the electron mobility in GaAs is a factor of 3 higher than in silicon. Thus, for comparable geometries, the intrinsic gain for a GaAs device will be substantially higher than for a silicon device.

The cell design and geometry configuration of power GaAs FETs follow design rules similar to those used by designers of silicon bipolar devices. Figure 5.5 shows the cross section of a power GaAs FET that uses air bridge construction and *via holes* to ground the source terminal of the FET. The gate length, seemingly a misnomer because it is shorter than the gate width, is the major parameter that determines device gain and hence operating frequency. Gate width is sometimes also referred to as the periphery. In general, it is desirable to use the largest gate length that permits sufficient gain at the operating frequency. This maximizes processing yield and hence minimizes component cost. Gate lengths for devices in the 1- to 30-GHz range may vary from 2.0 μm to as little as 0.25 μm. While frequency limits can be increased to some degree by decreasing the gate length, increases in power output require greater transistor gate width to support the increased current flow; however, if gate fingers are made too wide, the microwave signal will accumulate a phase shift and will be attenuated while propagating down the gate metal; consequently, the overall gain will be degraded. Total effective increases in gate width can be achieved by paralleling several adjacent gates in order to increase the total channel area per given area. This is similar to increasing emitter periphery per unit base area in the design of bipolar transistors. In addition, the structure must be designed to maintain as high a source-drain breakdown voltage as is possible in order to maximize power output capability. The output power capability of GaAs FETs increases almost linearly with increases in the total gate width, while the power gain decreases slowly with increasing total gate width. The maximum practical total gate width that can be accommodated on a single chip is limited by the following factors:

1. *Yield of the device:* A typical dc processing yield may be 0.995 per 100 μm of gate periphery. A 24-mm chip would therefore have an expected yield of only 30 percent.

2. *Difficulty of impedance matching:* Increases in power output are the result of adjacent channels being connected in parallel. For higher power levels, overall device impedances become lower and lower. For example, the real part of the input impedance for a 24-mm chip would be less than 1 ohm.

3. *Decrease of total power gain:* Uniform current distribution among gate fingers becomes increasingly difficult to manage as the number of paralleled gates increases. Combining inefficiencies result, and the overall device gain decreases.

4. *Physical device size:* The size of a 24-mm periphery chip would be approximately 3000 square mils (75 mils by 40 mils). Larger chip areas decrease the probable assembly yield because assembly difficulty increases with larger chips, greater numbers of wires, and larger packages.

5. *Dissipated power:* The thermal conductivity of GaAs is poor. The dissipated power from larger devices will result in extremely high channel temperatures on the die surface, and reliability will be impacted.

Silicon Power FETs. Silicon bipolar power transistors have been under development far longer than their silicon FET equivalents; consequently, many of the earliest solid-state transmitter designs utilized the bipolar devices. However, the silicon power FET is a viable alternative device type for the amplifier designer. Unlike bipolar transistors, which are minority carrier devices, FETs are

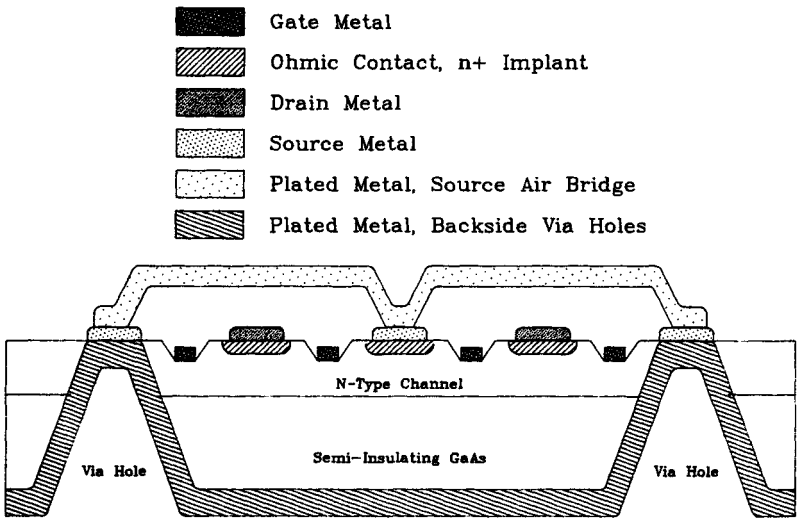


FIG. 5.5 Cross section of a GaAs power MESFET chip.

majority carrier devices and exhibit inherent thermal stability. In contrast, bipolar devices are minority carrier devices, and since minority carriers are thermally generated, bipolar power transistors tend to generate localized hot spots and can become thermally unstable. Resistive ballasting techniques used in both the collector and the emitter leads of a bipolar transistor reduce the intrinsic device gain and efficiency but offset the thermal-instability problem. In the power FET, however, large active cell areas can be combined without using these ballasting techniques and without experiencing the problems of thermal runaway.

In general, there are advantages that silicon FETs exhibit, namely,[8]

1. *Thermal stability:* This results from a negative temperature coefficient of power gain.

2. *Gain control ability:* Pulse shaping can be accomplished by using low power gate bias modulation.

3. *Ease of impedance matching:* This is particularly true for the static induction transistor (SIT), which can operate from dc supply voltages as high as 100 V and hence can provide higher impedance levels than other device types for a given power output level.

Millimeter-Wave Solid-State Power Sources. Solid-state power in the millimeter-wave frequency range is generated from low-power oscillators or negative-resistance amplifiers. The most promising results have been obtained from IMPATT diodes or Gunn diodes. However, TUNNETT (tunnel injection transit time) devices and BARITT (barrier injection transit time) devices are also used. When an extremely short gate length is used, a MESFET construction can be employed at these frequencies, but fundamental limitations on charge carrier velocities and processing tolerances on physically short gate lengths limit the practical operation of MESFET oscillators to below 50 GHz.

IMPATT diodes have been made from silicon, gallium arsenide (GaAs), or

indium phosphide (InP) and operate as millimeter-wave oscillators. Silicon devices offer the most promise because silicon provides the most efficient junction heat removal. Overall performance of the diode depends upon the doping density and the thicknesses of the epitaxial, junction, and interface layers. The level of power output from the devices depends upon whether the device is operated pulsed or CW but can range from 1 W CW at 80 GHz to approximately 20 W pulsed at 80 GHz.[9] In addition to IMPATT diodes, transferred electron devices (more commonly named Gunn diodes) made from GaAs or InP can be used up to about 100 GHz. At the lower part of the millimeter-wave band, CW power levels up to 2 W with 15 percent efficiency and pulsed power levels up to 5 W with 20 percent efficiency have been reported.

5.3 SOLID-STATE MICROWAVE DESIGN

The solution to the radar range equation for most applications invariably requires high peak and average radiated power from the antenna in order to ultimately maintain some minimum signal-to-noise ratio on receive. The impact on the solid-state transmitter designer of the requirement for high radiated power is fundamental: high power must be achieved by combining the outputs of lower-power amplifiers in order to develop the required radiated levels. The amplifier-combining approach generally takes one of two different configurations: space-combined or corporate-combined structures, as shown in Fig. 5.6; however, there are also hybrid approaches in which corporate-combined modules feed

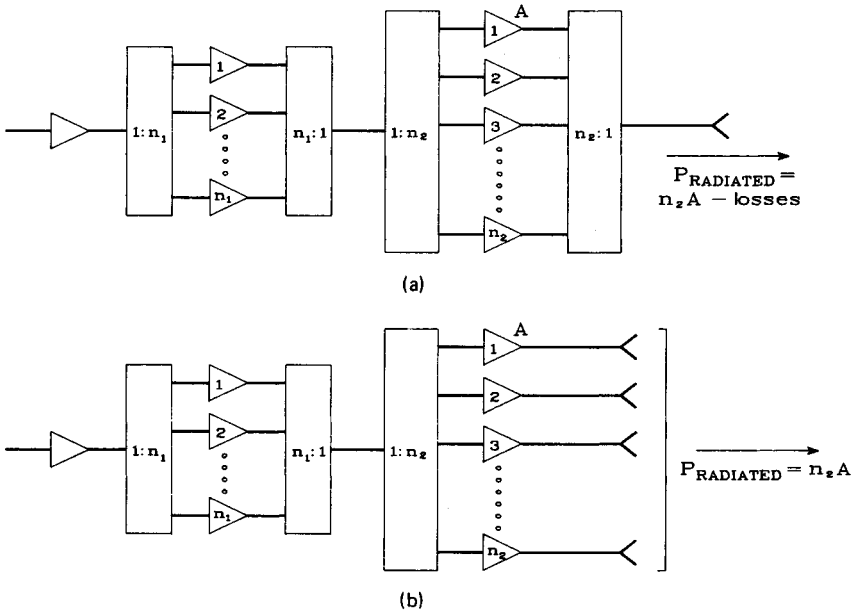
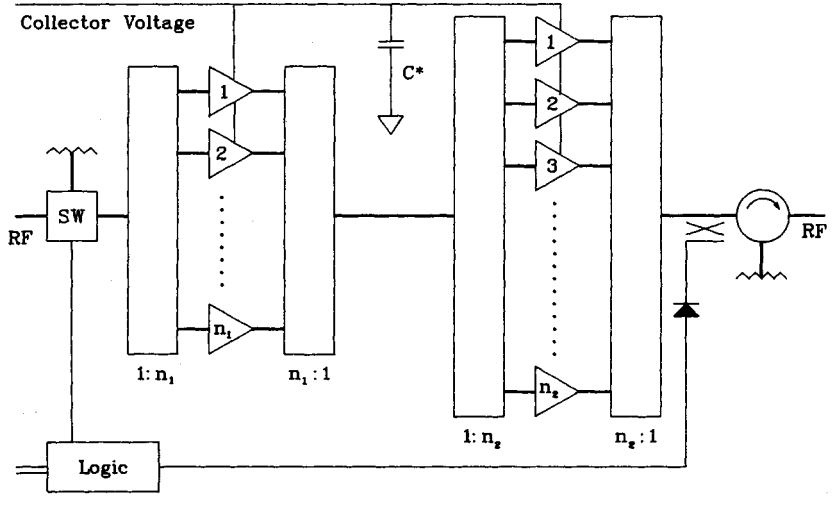


FIG. 5.6 Block diagram of (*a*) a corporate-combined power amplifier and (*b*) a space-combined power amplifier.

rows of a space-combined array. The phased array configuration is an example of the space-combined approach wherein each radiating antenna element is fed by an amplifier module and the wavefront is formed in space. An example of the corporate-combined design is a parabolic reflector antenna illuminated from a single feedhorn. The power radiated from the horn has been combined from the outputs of many amplifier modules. Solid-state transmitter designs have been built around each of these generic forms, and the components that are required in the implementation of each share similar characteristics and devices.

High-Power Amplifier Design. In the corporate-combined system, high power levels are generated at a single point by combining the outputs of many low-power amplifiers. The amplifier module is usually partitioned such that the required electrical performance is achieved while the constraints imposed by the mechanical, cooling, maintenance, repair, and reliability disciplines are simultaneously achieved. In general, a module, as shown in Fig. 5.7, consists of a number of identical amplifier stages that are parallel-combined and isolated from one another through the use of microwave combining and isolating techniques. Drive power for this parallel group is obtained from driver or predriver stages, using microwave power dividers. A circulator at the module output port is commonly used to protect the amplifier from the damaging effects of high-load VSWR, most notably from the antenna. Also, ancillary circuitry such as energy storage capacitance, built-in-test (BIT) sensors, or adaptive control components may be included.[10]

Single-Stage Characteristics. Transistors that operate in the HF through S-band frequency ranges are commonly biased either Class-B or Class-C. Class-C



C* : Energy storage capacitance for pulsed amplifiers

$$C = \frac{I \times dt}{dv}$$ where I = peak current, dt = pulse length, dv = pulse voltage droop

FIG. 5.7 Block diagram of a high-power solid-state amplifier module for a corporate-combined transmitter.

operation is the preferred mode since the RF output power of the amplifier is maximized for a given prime power input.[11,12] In general, the base-emitter junction is reverse-biased, and collector current is drawn for less than half of an RF cycle. Collector current is drawn only when the input voltage exceeds the reverse bias across the input and the output voltage is developed across a resonant-tuned load. The net result is high amplifier efficiency. The practical implications of a Class-C-biased amplifier stage are as follows:

1. No quiescent dc current is drawn while the device is not being driven, such as in the radar receive mode. Hence there is no power dissipation in the amplifier while the transmitter is operating in this mode.

2. Only one power supply voltage is necessary for the collector terminal of the transistor. The Class-C operation is a *self-bias*, wherein the transistor draws collector current only when the RF voltage swing on the input exceeds the built-in potential of the emitter-base junction. Additional reverse biasing may be introduced as a result of the voltage drop induced by current flow across parasitic resistance of the base or emitter bias return, and in common-base operation this will result in degraded power gain.

Unlike Class-A linear amplifiers, there are peculiar operating characteristics of the Class-C-biased amplifier that must be recognized in the overall amplifier design. Among these are the RF characteristics of the device as a function of varying RF input drive levels, varying collector voltage supply levels, or varying load impedance. As the RF input drive level of a Class-C-biased device is increased from zero, the dc potential of the reverse-biased base-emitter junction is surpassed and the device begins to draw collector current from the fixed dc supply voltage. The amplifier shows somewhat "linear" transfer characteristics as the drive is increased until the device begins to saturate. Eventually a point of saturated power output capability of the device is attained, and further increases in RF input drive level will actually produce a degraded power output level. At this point the device may also be thermally limited at a device junction. One of the characteristics of this mode of operation is that devices will continue to draw collector current as the amplifier is driven harder; consequently, there exists an optimum operating point with regard to RF drive level. This generally occurs as the transistor is driven approximately 0.5 to 0.75 dB into saturation.

At the chosen operating point and under the conditions of fixed RF input drive and fixed dc supply voltage, amplifiers of this type also exhibit sensitivities of insertion phase and power output to changes in the input drive level, collector voltage, temperature, and load impedance.[13] Some of the common sensitivities of a Class-C-biased amplifier are given in Table 5.3. Although a nominal 50-ohm load impedance may be assumed, the typical loading effect from the microwave power combiners and the circulator will produce variations in the load impedance presented to the transistor stage that may vary by ±50 percent from the nominal level. Depending on the phase of this mismatch, which can vary among adjacent devices, the port-to-port characteristics of an amplifier can vary dramatically. An important facet of Class-C design is that the response of the single-stage amplifier to these external perturbations must be addressed. Proper selection of the nominal load impedance directly affects the power output, gain, insertion phase, efficiency, and peak junction temperature of the single stage. Changes in the port-to-port insertion phase may result in combining inefficiencies among adjacent amplifiers since the RF power that is lost to the fourth-port termination of a microwave combiner, when adjacent amplifiers are combined, is given by

TABLE 5.3 Performance Sensitivities for a Class-C-Biased Amplifier

Parameter	Value
Amplitude sensitivity to RF drive	0.2–0.9 dB/dB*
Amplitude sensitivity to collector voltage	0.2–04 dB/V†
Phase sensitivity to RF drive	10–13°/dB
Phase sensitivity to collector voltage	0.5–1.5°/V
Phase runout	5–20°‡

*Function of the saturation level.
†Function of the collector voltage level.
‡Function of pulse length and transistor geometry.

$$\text{Power lost (dB down)} = 10 \log [(1 + \cos \theta)/2] \tag{5.1}$$

where θ is the phase difference between amplifiers. Finally, the long-term reliability of the amplifier may be affected by the choice of nominal load impedance since this affects the operating junction temperature of the transistors.

Module Design. In a very simple sense, the design of an amplifier module consists of matching the power transistors to the proper impedance level and then combining the power levels at these impedances. A typical packaged power transistor has low input and output impedances that must be transformed up to higher level, usually 50 ohms. Thus, the typical amplifier design task must address both low-loss and inexpensive reactive impedance-transforming networks that can provide the proper source and load impedances to the transistor. The common medium for providing this function is a microstrip transmission line. Microstrip is a quasi-TEM mode transmission-line medium that requires photolithographically defined lines on a low-loss, high-quality dielectric substrate. Reactive components that are necessary as impedance-matching elements can be approximated in the microstrip format. An inexpensive reactive matching network can be formed by using an interconnected pattern of microstrip elements. Shunt- and series-connected inductive reactances as well as shunt capacitive reactances are the most easily fabricated and most frequently used matching elements up through 10 GHz.

The outputs of identical single-stage power amplifiers are commonly summed by using splitting and combining techniques that also provide isolation between paralleled amplifiers. It is important to note that isolation is necessary between adjacent combined amplifier stages. Should one device fail, the power combiner must provide a constant load impedance to the remaining device. Half the power of the remaining active device, however, will be dissipated in the isolation resistor of the combiner.

A splitting-combining network must also provide serial isolation among amplifier stages as well as parallel isolation. As a Class-C-biased transistor is pulsed, it passes through its cutoff, linear, and saturation regions. Consequently, the input and output impedances are dynamically varying, and the input impedance changes most dramatically. The input impedance match may change from a near-infinite VSWR in the OFF state to a well-matched condition in the ON state. When amplifier stages are serially cascaded without any means of isolating successive stages, the changing input impedance will appear as a varying load impedance to the previous stage. This may very well send the previous stage into oscillation. Figure 5.8 illustrates splitting-combining configurations that provide the necessary isolation by utilizing reflected signal phase cancellation techniques.

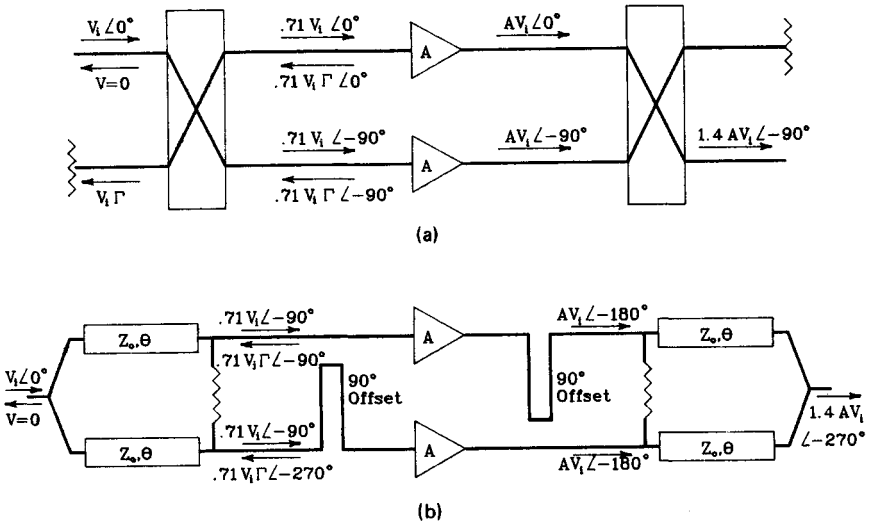


FIG. 5.8 Power amplifier combining configurations that provide minimum input port reflected power. (*a*) Quadrature-coupled amplifier pair. (*b*) Split-T amplifier pair with a 90° offset. (*Reprinted with permission from E. D. Ostroff et al., "Solid-State Transmitters," Artech House, Norwood, Mass., 1985.*)

Phased Array Transceiver Module Design. In contrast to the design of a corporate-combined output, where significant losses can accrue in the combining circuitry, the solid-state phased array system uses individual transceiver modules to feed antenna elements on an array face. Consequently, the phase shifting can be done at a low power level, where dissipated power levels in the phase shifters can be much smaller. The transceiver module, regardless of complexity, has four fundamental functions: (1) to provide gain and power output in the transmit mode, (2) to provide gain and low-noise figure in the receive mode, (3) to switch between transmit and receive states, and (4) to provide phase shift for beam steering in the transmit and receive states. A block diagram of a typical transceiver module is shown in Fig. 5.9.

Microwave Monolithic Integrated Circuits. The use of integrated circuits in transceiver designs has enabled bold new module configurations, and hence phased array systems, to be envisioned. Since some of the more complex functions in the generic transceiver block diagram can be fabricated by using MMIC technology, the components that can be realized through the use of this technology can be employed to create system architectures that are difficult if not impossible to design with other, less integrated technologies. The MMIC design approach utilizes active and passive devices that have been manufactured by using a single process. Active and passive circuit elements are formed on a semi-insulating semiconducter substrate, commonly GaAs, through various deposition schemes. The monolithic approach to circuit design inherently offers several advantages:

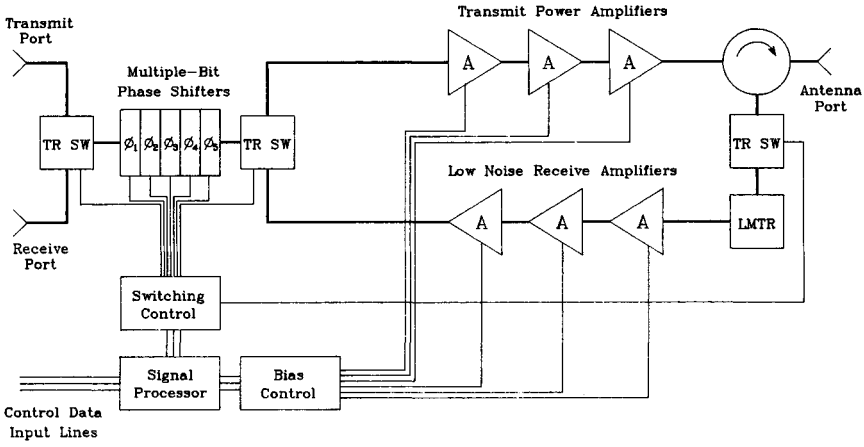


FIG. 5.9 Block diagram of a generic transceiver module for phased array radar.

1. *Low-cost circuitry:* Component assembly is eliminated since complex circuit configurations using both active and passive components are batch-processed on the same substrate.

2. *Increased reliability:* Batch-processed components lead to a reduced number of parts, from the reliability standpoint, and hence to increased reliability.

3. *Increased reproducibility:* Circuitry that is batch-processed or circuits that originate from the same wafer exhibit consistent electrical characteristics from component to component.

4. *Small size and weight:* Integration of active and passive components onto a single chip results in high-density circuitry with multiple functions on a single chip. Overall, the transceiver module can be made much smaller than with discrete components.

However, there are inherent drawbacks to the MMIC approach to component design. The nonrecurring engineering design cost is very high. A typical multistage low-noise amplifier chip design, for example, may easily consume a year's worth of effort before a final design is realized. The cost of wafers and the processing costs in general are very high, such that low-yielding circuit designs may still result in high-cost components. Little circuit trimming can be accommodated in the MMIC approach; consequently, designs must be made tolerant to processing variations or lower performance standards must be accepted for a given design.

The typical processing construction sequence for a GaAs MMIC chip is fairly similar among the GaAs foundries.[14] The active channel region of an FET is delineated by any of several patterning techniques on a semi-insulating GaAs substrate. A combination of deposited dielectric films and metal layers is used to form the passive components and also to interconnect all the elements of the circuit. Standard libraries of circuit elements may include FETs (used as linear amplifiers, low-noise amplifiers, saturating power amplifiers, or switches), resistors, capacitors, inductors, diodes, transmission lines, interconnects, and plated ground vias.

Monolithic circuit elements can be viewed as consuming real estate on a GaAs substrate, and the processing complexity of each step determines the relative yield for individual elements. Although typical processing yields for FET devices may exceed 95 percent per millimeter of gate periphery and greater than 99 percent per picofarad of capacitance, the net yield for a complex circuit may be quite low. For example, a four-stage power amplifier chip that is capable of 3 W of power output at 2 GHz may require more than 9 mm of total gate periphery and may have a total of 75 pF of blocking, bypassing, and matching capacitance. The overall dc yield for this device may be as low as 30 percent when the processing yields for each step are accounted for; high-reliability screening that addresses visually detected imperfections may reduce that yield again by half.

Transceiver Module Performance Characteristics. The partitioning of transceiver module circuit functions onto GaAs chips usually represents a tradeoff among several design issues, and the resultant circuit configurations represent a compromise among the goals of optimum RF performance, high levels of integration, and fabrication yields that are consistent with processing capabilities of GaAs MMICs. Among the single-chip circuit designs that have been reported from UHF through millimeter-wave frequencies are power amplifiers, low-noise amplifiers, wideband amplifiers, phase shifters, attenuators, T/R switches, and other special function designs.

Component Characteristics. Performance characteristics for monolithic circuits vary significantly and are the result of processing variations, layout considerations, yield optimization, or circuit complexity. However, the design tradeoffs have resulted in commonly partitioned circuits. Some of the design criteria or characteristics peculiar to amplifiers and other circuits as follows:

LOW-NOISE AMPLIFIERS. (1) Multiple-stage linear designs require proper device sizing of successive stages in order to maintain low intermodulation distortion products. (2) Circuit losses on the input, before the first stage, degrade the noise figure of the design; therefore some designs utilize off-chip matching. (3) A low noise-figure requires a bias condition that is close to the pinch-off voltage of the FET. Both gain and noise figure are highly dependent on the pinch-off voltage when the FET is biased close to pinch-off. Since the pinch-off voltage can vary significantly for devices from the same wafer, the bias condition must be chosen carefully. Gain and noise figures are usually traded off against repeatable performance.

POWER AMPLIFIERS. (1) Total gate periphery is usually at a premium. For high-power design, the load impedance presented to the final device must be carefully chosen such that power output and efficiency are maximized. (2) Losses in the output circuit of the final stage can significantly reduce power output and efficiency. Off-chip matching may be necessary to maximize power output for a given design. (3) GaAs is a poor thermal conductor. Power FET design that addresses thermal management is required. Adequate heat sinking of the chip is mandatory. (4) For efficient multiple-stage designs, it is necessary that the final stage of the amplifier reach saturation before the preceding stages. This must be addressed in the circuit design.

T/R SWITCHING. (1) For switching applications, the FET design should be chosen such that the ratio of OFF-ON resistance of the FET is kept as high as possible. The channel length largely determines the ON resistance and hence the insertion loss of the device. The tradeoff between short gate length (thus lower processing yield) and insertion loss must be examined. (2) The value of the parasitic drain-source capacitance will affect the OFF-state isolation of the device. This capacitance depends largely on the source-drain spacing of the FET geometry. Critical

applications are usually only the front-end switching configurations in a transceiver module, i.e., before the receive low-noise amplifier or after the transmit amplifier.

PHASE SHIFTERS. (1) Phase-shifter designs generally utilize either a switched-line or a loaded-line circuit configuration, using either distributed transmission-line components or lumped-element equivalent circuits, to achieve multiple-bit phase shifting. Switched-line configurations rely on FET switches to switch lengths of transmission line in and out of the circuit and are typically used for higher frequencies where less chip area is needed. Loaded-line configurations use the switched FET parasitics as circuit elements to introduce the necessary phase changes.

The photograph of a representative MMIC chip, shown in Fig. 5.10, is a 12-W power amplifier chip pair that operates at S band. The final stages of this particular design use FETs with a total of 30-mm gate periphery.

Module Characteristics. Performance data exists for modules that use GaAs MMIC technology in the 1- to 10-GHz frequency range. Animated interest in lightweight, adaptive array applications will continue to push this technology. The reported performance characteristics of transceiver modules are generally a combination of multiple MMIC chip configurations and/or multiple-chip configurations with additional hybrid components to augment the performance of the GaAs components. In addition, the complexity of the transmit/receive functions varies among the module configurations. Data for various modules is enumerated in Table 5.4.[15,16,17] An integrated transceiver module that operates in the X-band frequency range is shown in Fig. 5.11.

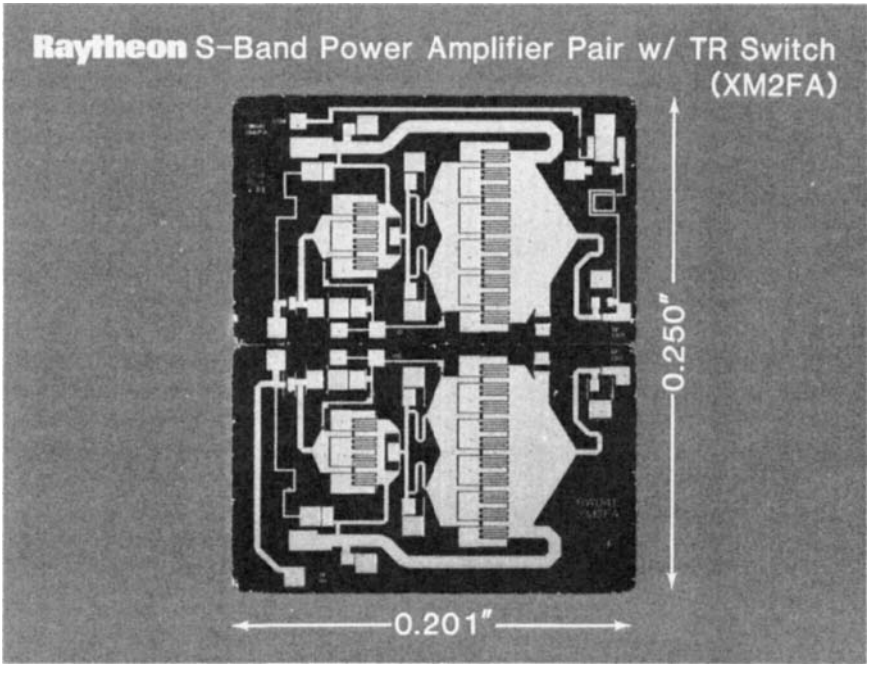


FIG. 5.10 An S-band 12-W GaAs power amplifier MMIC chip pair. (*Photograph courtesy of Raytheon Company.*)

TABLE 5.4 Integrated Transceiver Module Performance Characteristics and Sensitivities

Performance characteristics

Frequency	Transmit mode: RF power, W	Transmit mode: Gain, dB	Transmit mode: Efficiency, percent	Receive mode: Gain, dB	Receive mode: Noise figure, dB	Receive mode: rms phase error: Gain, dB	Receive mode: rms phase error: Phase, deg	Size, in^3	weight, oz
L band*	11	35	30	30	3.0	0.8	5.0	4.0	4.0
S band	10	31	16	25	4.1	0.5	4.0	2.4	2.4
S band	2	23	22	27	3.8	N.A.	4.6	2.9	3.6
S/X band†	2	30	25	...	...	...	...	0.25	N.A.
X band	2.5	30	15	22	4.0	0.6	6.0	0.7	0.7

Performance sensitivities

Parameter	Transmit	Receive
Gain sensitivity to drain voltage	1 dB/V	1 dB/V
Phase sensitivity to drain voltage	4°/V	2°/V

*Includes hybrid stage on transmit output and receive input.
†Transmit amplifier only.

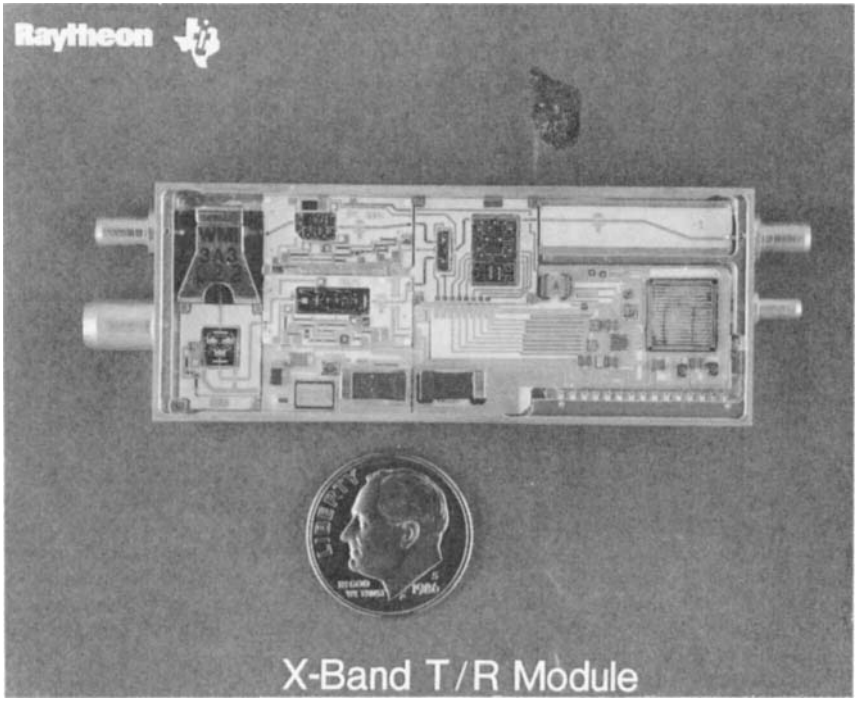


FIG. 5.11 An integrated X-band transceiver module. (*Photograph courtesy of Raytheon Company/Texas Instruments; development work sponsored by RADC, Griffiss Air Force Base.*)

5.4 TRANSMITTER SYSTEM DESIGN

Solid-state amplifiers are usually used in space-combined configurations, corporate-combined configurations, or a hybrid combination of the two. The advantages of solid-state in transmitter applications have already been noted, and some of the performance nuances are noted in the following paragraphs.

Performance Sensitivities

Peak and Average Power Differences. A significant difference between the optimum operating characteristics of solid-state amplifiers and tube amplifiers is that transistors are average-power devices while tubes typically are peak-power devices. The operating characteristics that result from this difference have tremendous impact on the overall system design. The peak power output of microwave transistors is limited by electrical characteristics, while the average power output capability is determined by thermal layout of the transistor. Transistors can be designed to operate for short (< 10 μs), medium (10 to 150 μs), or long (> 150 μs) pulse widths and for duty cycle ranges to CW. Unlike tubes, where the ratio of peak to average power capability can be very high, the peak power output capability of a transistor operated in a short-pulse low-duty mode may only be 2 to 3 times greater than the peak power capability when that device is operated CW. Thus, solid-state operation favors long pulse widths and high duty cycles. For retrofit systems, where high peak power from a short pulse width is required, the acquisition cost of a solid-state transmitter may be prohibitive. The cost of the transmitter may ultimately be reduced if the waveform can be altered to favor higher duty cycle, since the cost in dollars per average watt of the transistor becomes lower as the duty cycle is increased. As long as this cost differential is large enough to offset the added cost in signal processing to accommodate long pulses, a less costly transmitter may be realized.

Amplitude and Phase Sensitivities. Transistor amplifiers that utilize Class-C-biased devices exhibit sensitivity to RF drive level that may degrade the output pulse characteristics. The single-stage amplifier will typically exhibit a very narrow "linear" transfer characteristic; the linear region may exist over only a narrow 1- to 3-dB window. This becomes strikingly critical when several Class-C-biased stages are cascaded in series, as is common in most amplifier configurations. The final tier of output transistors in a serial amplifier chain must be driven into saturation by the preceding stages, and the drive level must be held relatively constant as a function of time and temperature. Since these devices show a narrow operating range, small decreases in the input RF drive level to a multistage amplifier may bring the final tier of devices out of saturation. The net result is an unacceptably degraded output pulse fidelity. One solution has involved a feedback path from a drive-level monitoring point to a variable power supply voltage that maintains the drive level within a specified range for various operating conditions.[10]

In addition to the problems associated with pulse envelope distortions, the phase and amplitude sensitivity of transistor amplifiers to power supply ripple may impact the MTI improvement factor that can be attained. The sensitivities of amplifier stages have already been described. In a multistage amplifier the phase errors due to power supply sensitivity of serially cascaded stages will add, and the limit on MTI improvement factor is

$$I = 20 \log d\theta \tag{5.2}$$

where $d\theta$ is the magnitude of the insertion phase ripple. The corresponding limit on improvement factor caused by amplifier amplitude instability is

$$I = 20 \log (dA/A) \tag{5.3}$$

where dA and A are the amplitude ripple and the magnitude of the amplitude voltage, respectively.

Time jitter of the RF output pulse envelope can also result from power supply ripple, as a result of Class-C operation of the module, and will also limit the MTI improvement factor. The limitation from this effect is

$$I = 20 \log (dt/T) \tag{5.4}$$

where dt is the time jitter and T is the pulse width. If pulse compression is used, T is still the transmitted-pulse width, not the compressed-pulse width.

In addition, careful design must take into account interactions that can occur as a result of the many cascaded stages of solid-state amplification. These include the following:

1. Phase errors in cascaded stages simply add. However, it may also be possible to arrange them to cancel by proper phasing of power supply ripples for different stages. Similarly, in a stage with N modules in parallel, each with its own high-frequency power-conditioned power supply, the overall phase ripple can usually be assumed to be reduced by a factor equal to the square root of N if the power supply clocks are purposely not synchronized.

2. Because of saturation effects amplitude errors in cascaded stages do not simply add. However, amplitude errors in driving stages will cause drive-induced phase variations in the following stages, as noted above, all of which must be counted.

3. Time jitter in cascaded stages simply adds unless they are arranged to cancel or to be root-sum-squared, as discussed in Par. 1. In addition, amplitude fluctuations in the RF drive will also cause drive-induced jitter, which may even exceed power-supply-ripple-induced jitter, so this factor must be carefully measured.

Spectral Emissions. As a result of Class-C-biased amplifier operation, when a rectangular RF drive pulse is applied to a module, the amplifier will typically show rise and fall times that are on the order of nanoseconds. The output signal spectrum of this pulse shape may not meet spectral emissions requirements, and it may be necessary to slow the rise and fall times. This becomes very difficult when stages are serially cascaded. Because of the highly nonlinear effect described in the preceding subsection, each Class-C stage tends to speed up the rise and fall times of the driving pulse. Consequently, an input pulse shape with slow rise and fall times may be necessary to achieve the desired output-pulse spectral composition.

Control of the rise and fall times is complicated by the necessary use of external bias injection networks. The pulse fall times are generally very fast, on the order of nanoseconds. However, the rise time for a high-power transistor amplifier may be slower, on the order of 100 nanoseconds, and is the result of the reverse biasing that may be encountered by instantaneous current flow in the emitter bias return as the transistor is turning on. This is a design problem for common-base operation, but a common-base configuration is often necessary

since it provides more power gain than common-emitter operation at frequencies above approximately 1 GHz.

Power Combining. To achieve very high levels of output power from a single port, combining the outputs of a large number of modules is required, and therefore a complex combining design is necessary. A power combiner coherently adds together the RF output voltages of individual modules and delivers to a single port the sum total of the modules' output power, minus the losses of the combiner. There are several power combiner-splitter configurations available to the module circuit designer, and all display somewhat varied characteristics.[18] In general, the requirements for a power combiner are:

1. The combiner should have low insertion loss, such that transmitter power output and efficiency are not compromised.
2. The combiner should have RF isolation among ports, such that failed modules do not affect the load impedances or combining efficiency for the remaining functioning modules.
3. The combiner should provide a controlled RF impedance to the amplifier modules, such that the amplifier characteristics are not degraded.
4. The combiner reliability should far exceed the reliability of other transmitter components.
5. The dissipated power capability of the power combiner terminations should be sufficient to accommodate any combination of power amplifier failures.
6. The mechanical packaging of the power combiner should allow modules to be repaired easily. The packaging should also provide short, equal phase and low-loss interconnections between the amplifier modules and the combiner.

High-power combiners may be either reactive or hybrid (or equivalent magic-T) designs. In the hybrid design, any imbalance or difference between the phase and amplitude of the voltages that are being combined is directed to a resistive termination. The net result is that a constant load impedance is presented to the amplifier module under all conditions even when an adjacent module in a combining tier has failed. In a reactive combiner design, any imbalance in power or phase between two input signals results in reflected power and increased VSWR to the module driving it. Power amplifier modules that are not protected from high-load VSWR can be damaged by reflected power from the combiner. In addition, frequency-dependent phase and amplitude ripple may result from this configuration.

Typical RF transmission media that are used in the construction of high-power combiners include coaxial transmission lines, microstrip or stripline transmission lines, or waveguide. The choice of transmission medium is generally a function of many parameters, including peak and average power-handling capability, operating frequency and bandwidth, mechanical packaging constraints, and, of course, the overall loss that can be tolerated. More often than not a combiner design utilizes a hierarchy of cascaded designs to sum the outputs of many modules;[10] however, unique configurations that sum many ports to a single port have been built.[19,20,21]

Solid-State Transmitter Design Examples

AN/TPS-59. The AN/TPS-59 (Sec. 20.1) is a solid-state, L-band, long-range, 3D air defense surveillance radar developed for the Marine Corps by the Elec-

tronic Systems Division of the General Electric Company.[22] The radar is tactically mobile and consists of a trailer-mounted rotating antenna and two radar shelters. The shelters house the digital signal processor, waveform generator, preprocessor, computer, peripherals, and display consoles. One additional shelter is provided for maintenance aids. Radar surveillance coverage encompasses a volume out to 300 nmi and up to 100,000 ft with a 90 percent probability of detection within 200 nmi for a 1-m^2 fluctuating target. The search volume is scanned mechanically in azimuth through 360° and electronically in elevation through 20°. The rotating 15-ft by 30-ft antenna structure houses 54 row transceivers, each of which drives an RF distribution board that feeds one row of 24 dipole antenna elements. The peak power output capability of the system is 54 kW at an average duty cycle of 18 percent.

The row electronics circuitry feeds each of 54 row feed networks. The row electronics consists of transmit preamplifiers, transmit amplifiers, phase shifters, circulator, and logic control. There are ten 100-W transmit amplifier modules in the final output stage of the row electronics circuitry. Each power amplifier consists of two 55-W silicon bipolar power transistors driven by a smaller 25-W device. The 55-W transistors provide a minimum of nearly 7.0-dB gain from 1215 through 1400 MHz from a 28-V dc power supply. All three devices are beryllia-based transistors that are soldered into a metal-ceramic hermetic enclosure, a photograph of which is shown in Fig. 5.12.

Variants of this system were sold by General Electric to the North Atlantic Treaty Organization (NATO) as the GE-592 and to the U.S. Air Force as the AN/

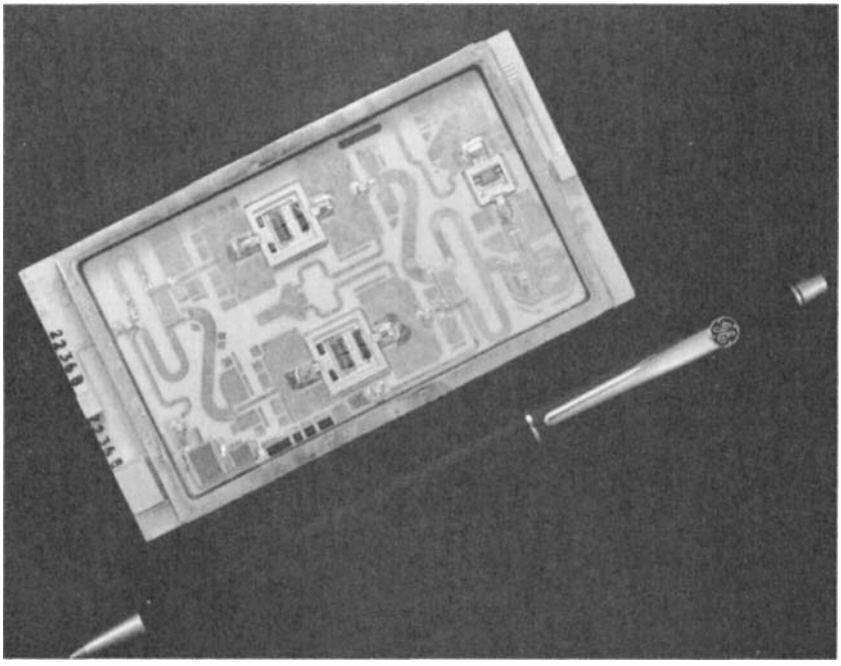


FIG. 5.12 AN/TPS-59 transmitter amplifier module. (*Photograph courtesy of General Electric Company.*)

FPS-117. The AN/FPS-117 radars are operational for the U.S. Air Force in Alaska (SEEK IGLOO Program), northern Canada (North Warning Program), and Berlin. The radar is also in use in Korea, for NATO in Iceland, and for Saudi Arabia as part of the Peace Shield Program. MTBF for these radars has been demonstrated to exceed the 1076-h specification, and more than 750,000 h MTBF has been demonstrated for the 100-W solid-state RF power amplifier modules.

PAVE PAWS. The PAVE PAWS (AN/FPS-115) system is a UHF solid-state active aperture phased array radar that was built for the Electronic Systems Division of the U.S. Air Force by the Equipment Division of the Raytheon Company.[23] The radar is a long-range system with a primary mission to detect and track sea-launched ballistic missiles. The radar uses 1792 active transceiver modules per face to feed dipole antenna elements. Extra elements and a narrow beam are used on receive, and upgrade capability has been included for the future installation of up to 5354 transceiver modules per array face. The peak power output from each face of the baseline system is 600 kW, and the average power output is 150 kW.

Among the 1792 modules per face, groups of 32 transceiver modules are operated as a subarray. In transmit, a high-power array predriver is used to drive 56 subarray driver amplifiers. Each of these power amplifiers provides enough RF drive for all 32 modules in one subarray. In receive, the signal from each of the 56 subarrays is fed into a receive beamforming network.

The transceiver module contains predriver, driver, and final transmit output stages, transmit/receive switching, low-noise amplifiers, limiter, phase shifters, and logic control. The transceiver module block diagram is shown in Fig. 5.13, and a photograph is shown in Fig. 5.14. The transmitter portion of the T/R module contains seven silicon bipolar power transistors, operated Class-C from a +31-V dc power supply. The amplifier is a 1-2-4 configuration, and each of the four final stages delivers 110 W peak for 16-ms pulse widths at duty cycles up to 25 percent. Table 5.5 enumerates some of the salient measured performance

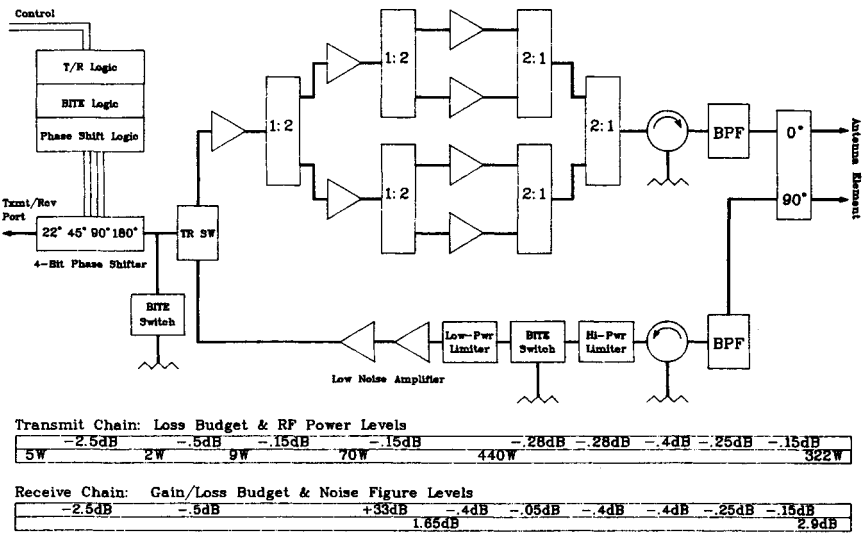


FIG. 5.13 Block diagram of the PAVE PAWS transceiver module.

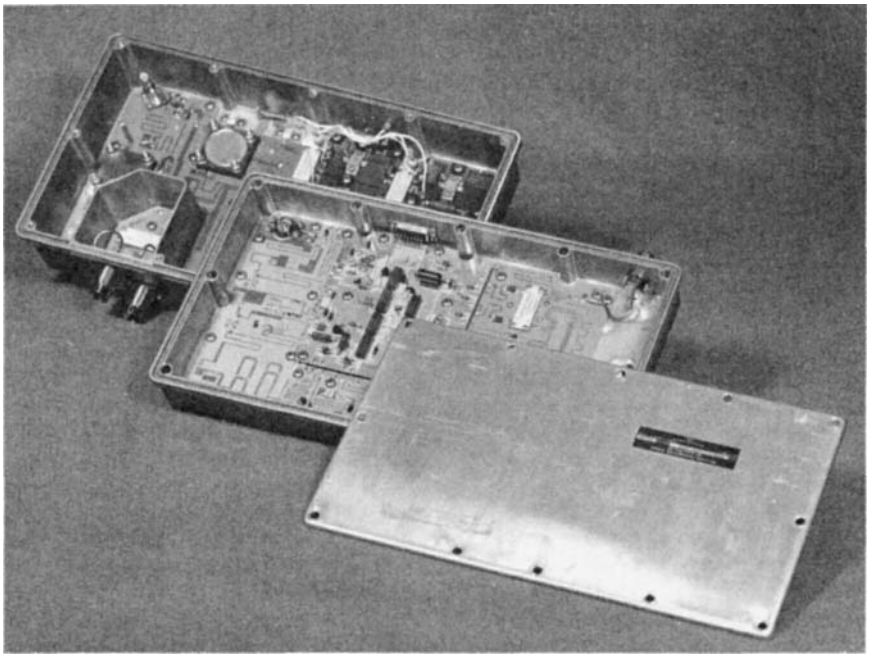


FIG. 5.14 PAVE PAWS transceiver module. (*Photograph courtesy of Raytheon Company.*)

TABLE 5.5 PAVE PAWS Solid-State Transceiver Module Performance*

Parameter	Performance	Specification
Peak power output	330 W	322 W
Output power tracking	0.24 dB rms	0.58 dB rms
Transmit phase tracking	6.7° rms	14° rms
Transmit phase-shifter error	2.52° rms	4.6° rms
Receive phase-shifter error	2.30° rms	4.6° rms
Efficiency	37.9 percent	36 percent
Receive gain	34 dB	27 dB
Receive gain tracking	0.57 dB rms	0.81 dB rms
Receive phase tracking	5.56° rms	10° rms
Noise figure	2.71 dB rms	2.9 dB rms

*Reprinted with permission from D. J. Hoft, Solid-State Transmit/Receive Module for the PAVE PAWS Phase Array Radar, *Microwave J.*, Horizon House, Norwood, Mass., October 1978.

NOTE: Frequency: 420–450 MHz; pulse width: 0.25–16 ms; duty cycle: 0–25 percent.

characteristics of the module. More than 180,000 transistors have been built into more than 25,000 modules.

AN/SPS-40. The AN/SPS-40 was an existing UHF, tube-type, long-range, 2D shipboard search radar system, for which a new solid-state transmitter, built for the Naval Sea Systems Command by the Westinghouse Electric Corporation, replaced the tube transmitter.[10] The existing waveform from the original trans-

mitter was not changed, and the solid-state unit was installed as a direct retrofit. This was not quite as difficult as usual, because the tube-type system already used long pulses and pulse compression, with a duty cycle of nearly 2 percent, which is a lot higher than older 0.1 percent duty cycle systems. Although it may have been desirable to go to a higher duty cycle and lower peak power to make the solid-state retrofit easier, the Navy preferred not to have to modify the rest of the system.

The 250-kW peak power transmitter uses a total of 128 high-power amplifier modules, which, along with power combining, predrivers, drivers, and control circuitry, are housed in three separate cabinets. There are 112 final power output modules arranged in two groups of 56. Each module produces 2500 W peak and 50 W average for a 60-μs pulse width at a 2 percent duty cycle. Drive power for the two banks of final output modules, 17.5 kW, is provided from the combined outputs of 12 more identical modules in the driver group. Predrivers and a redundant preamplifier are used as preceding drive stages.

The power amplifier module consists of 10 identical silicon bipolar power transistors arranged in a 2-driving-8 amplifier configuration to develop more than 2500-W peak power output over the 400- to 450-MHz frequency bandwidth. A photograph of the transmitter module is shown in Fig. 5.15. Each transistor is a 400-W peak-power device that is operated in a balanced push-pull circuit design. By using a push-pull configuration, the circuit designers have alleviated some of the low-impedance-matching problems normally associated with very high power transistors. The RF input drive to the module is 120 W peak and is used to drive two devices. A combined power level of greater than 600 W is split eight ways and drives the eight identical output stages. Losses in the output circulator, final power combining, and the fault detection circuitry reduce the combined power level to 2500 W. Output modules are liquid-cooled for normal operation, but an emergency backup forced-air cooling is provided in the event of a primary-cooling-system failure. The dissipated heat can be tolerated because the system operates at a low duty cycle.

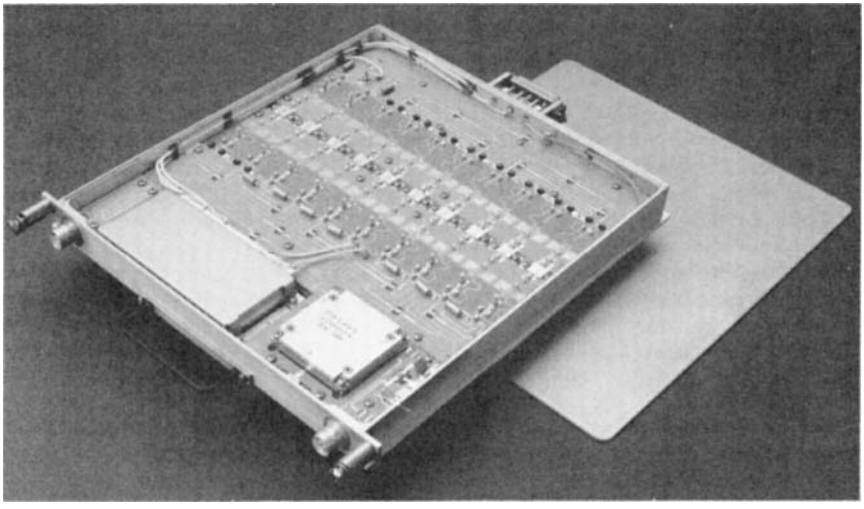


FIG. 5.15 AN/SPS-40 transmitter amplifier module. (*Photograph courtesy of Westinghouse Electric Corporation.*)

The power combining for each output cabinet consists of 56:1 combiners. The reactive power combiner consists of seven groups of 8:1 combiners fabricated in air stripline using 0.5-in ground-plane spacing. The seven outputs are combined by using a single 7:1 air stripline combiner with 1.0-in ground-plane spacing. The 130-kW outputs of the two 56:1 combiners are combined in a single 2:1 isolated hybrid that is manufactured by using 3⅛-in coaxial transmission line. The advertised losses of the 2:1 and 56:1 combiners are 0.1 dB and 0.25 dB, respectively.

Other features of the system include a self-monitoring and self-adjusting driver group power output level. The output level is monitored, and changes to the programmable 24- to 40-V dc power supplies maintain a constant driver group output level as a function of time and temperature.

NAVSPASUR. The solid-state transmitter for the Naval Space Surveillance System (NAVSPASUR) was designed and built by the Equipment Division of the Raytheon Company.[24] The NAVSPASUR is a CW radar, operating at 217 MHz, and is used to provide detection and track data on satellites and other objects as they pass over the continental United States. The solid-state transmitter was procured as a direct replacement for the prior tube-type version. This system produces a very high average power output (850 kW), and with the antenna gain of the system it produces an effective radiated power of over 98 dBW.

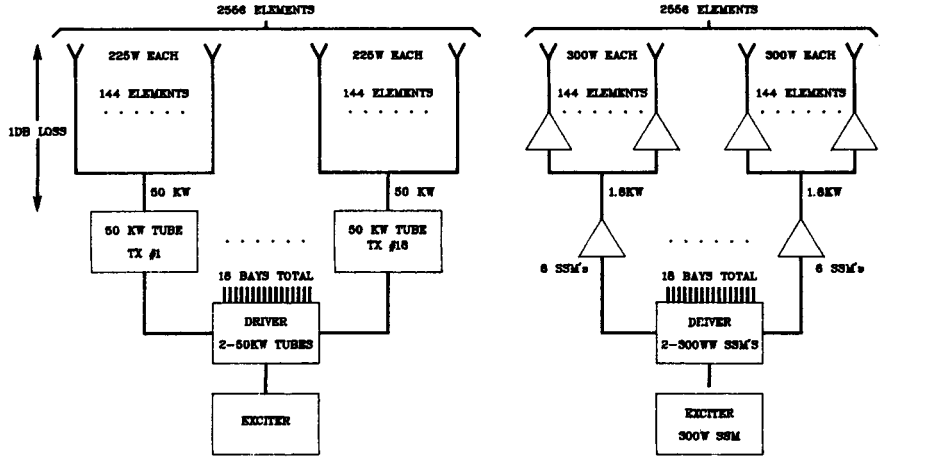
There is one main transmitter site at Lake Kickapoo, Texas, with smaller auxiliary sites in Gila River, Arizona, and Jordan Lake, Alabama. The transmitter sites are phased array dipole antennas driven through a coaxial corporate-feed system. The main transmitter site at Lake Kickapoo consists of 2556 antenna elements, each driven by a 300-W solid-state module located directly below the antenna. The most apparent advantages that the solid-state system has over the former tube version are:

1. Much lower dissipation is experienced in the corporate feed because the modules are colocated with the antenna. As a result, the overall site efficiency has been nearly doubled, thus contributing to lower life-cycle costs.

2. A fault-tolerant architecture has led to a system availability of near unity. With a module MTBF of 100,000 h, the maintenance for failed modules can be neglected for nearly 2 years before the transmitter power output degrades by 1 dB. Figure 5.16 illustrates the comparison between the original tube system and the solid-state retrofit.

The solid-state module is a 300-W CW amplifier that uses a 1-driving-4 configuration of silicon bipolar transistors operated common-emitter by using Class-C bias and a 28-V dc power supply. The operating characteristics of the module are delineated in Table 5.6, and Figs. 5.17 and 5.18 are a photograph and a block diagram, respectively. An input power level of 6.2 W is required to drive the module into saturation at the 300-W level. The module dissipates 200 W to the baseplate, which is convection- and radiation-cooled in the outdoor environment. Other module features include automatic fault detection and shutoff, harmonic filtering, and factory-adjustable delay line for module insertion phase matching.

RAMP. The RAMP (Radar Modernization Project) radar system is an L-band system built by the Raytheon Company to replace the earlier primary and secondary surveillance radars used for air traffic control by Canada's Ministry of Transport.[25,26] The primary surveillance radar consists of a rotating reflector, horn-fed by a solid-state transmitter, and redundant receive channels with receiver-exciters and signal processors. The primary surveillance radar operates



Before (tube system) After (solid-state system)

Transmitted power	576 kW	767 kW
Transmission efficiency	80%	95.9%
Maximum power in coaxial	40 kW	1.8 kW
Overall site efficiency	26.4%	52.6%
Site availability	0.8	0.9998

FIG. 5.16 NAVSPASUR transmitter design tradeoffs.

TABLE 5.6 NAVSPASUR Solid-State Power Amplifier Module Performance

Parameter	Performance	Specification
Frequency	216.98 MHz	216.98 MHz
RF power output (CW)	320.0 W	300 W + 0.5 dB
Gain	17.1 dB	16.8 dB
Spurious RF output (near-in)	−75 dBc	−70 dBc maximum
Spurious RF output (far-out)	−85 dBc	− 80 dBc maximum
RF dc efficiency	61.5 percent	58 percent minimum
Input return loss	14 dB	14 dB
Power output similarity (1σ)	0.29 dB	0.5 dB
Phase similarity (1σ)	3.0°	3°
DC voltages	28 V/16.5 A and 8.9 V/0.18 A	28 V/19 A and 8.9 V/0.2 A
Size	21 × 16 × 4.3 in	21 × 26 × 4.3 in
Weight	47 lb	47 lb
Operating ambient temperatures	0–116°F	0–116°F
Pressurization	5 lb/in^2	5 lb/in^2

between 1250 and 1350 MHz with a 25-kW peak power output and provides radar coverage to 80 nmi and to an altitude of 23,000 ft with an 80 percent probability of detection for a 2-m^2 target; with azimuth and range resolution to 2.25° and 0.25 nmi, respectively. The receiver-exciter efficiently utilizes the transmitter solid-state devices with a high-duty-cycle waveform. A double-pulse pair is used in the frequency-agile system, and target returns are processed by a four-pulse moving-target detector. The pulse pair consists of a 1-μs CW pulse that provides cover-

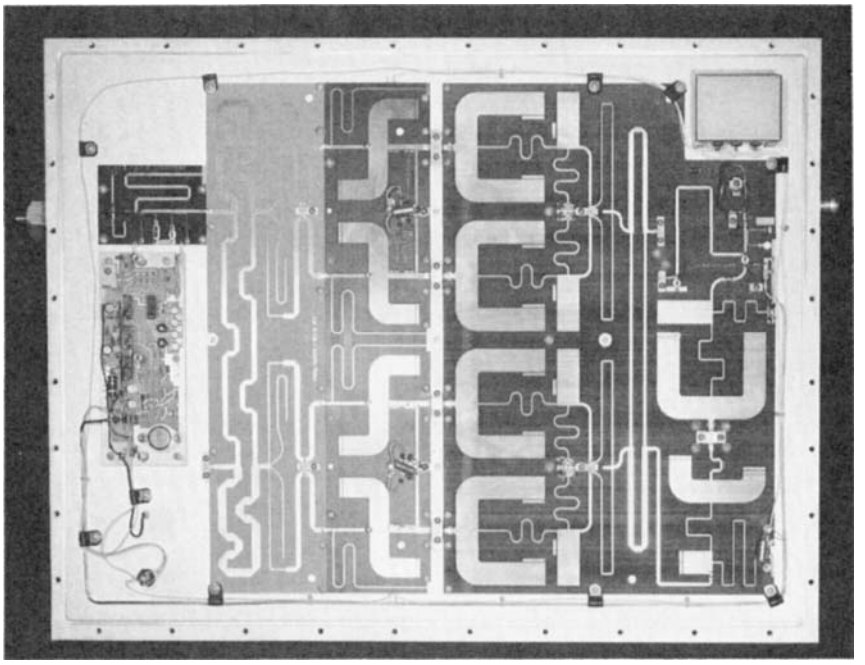
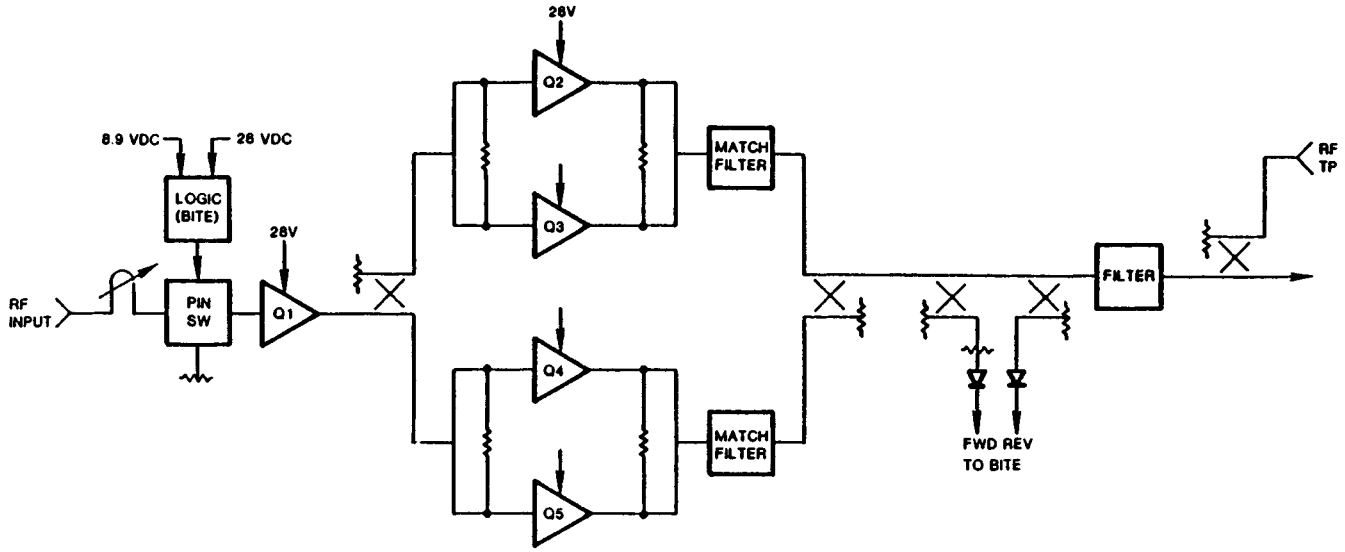


FIG. 5.17 NAVSPASUR transmitter amplifier module. (*Photograph courtesy of Raytheon Company.*)

age to 8 nmi and a 100-μs nonlinear chirp pulse that provides coverage to 80 nmi. The 100-μs pulse is compressed to 1 μs such that high duty cycle is achieved without compromising range resolution.

The transmitter consists of 14 modules, each capable of 2000-W power output, that are combined to produce the greater than 25-kW peak level. Two modules and a 33-V dc power supply make up a single transmitting group. The module consists of a 2-8-32 amplifier configuration of silicon bipolar power transistors. The 32 final output devices and the eight driver devices are 100-W transistors capable of operating up to a 10 percent duty cycle over the 100-MHz bandwidth at collector efficiencies greater than 52 percent. Each module is air-cooled, and the measured efficiency is greater than 25 percent when the module is operating at an 8.2 percent average duty cycle. Module power gain is greater than 16 dB. Figure 5.19 shows a photograph of the 50-lb module and the lineup of power transistors down the center spine of the module. A circulator is used on the output port to protect the 100-W devices from antenna-generated reflections, and control circuitry has been included to switch off modules in the event of cooling-system failure. A 14:1 high-power replicated combiner,[21] built by using a combination of reactive and resistive power-combining techniques in air dielectric stripline, is employed to sum the module outputs to the 25-kW level.



	BITE MONITOR	RF SWITCH	DRIVER	BRANCH-LINE 3-dB DIVIDER	3-dB WILKINSON	FINALS	3-dB COMBINER / FILTER (WILKINSON)	BRANCH-LINE COMBINER	BITE MONITORS	PRODUCTION TOLERANCE	
		−0.5	+9.70	−0.30	−0.20	+9.2	−0.06(−0.2)	−0.10	−0.03	−0.60	Gain/loss (dB)
6.2		5.7		52		11.5	(4x94)		344	300	Power (watts)

FIG. 5.18 Block diagram of the NAVSPASUR transmitter amplifier module.

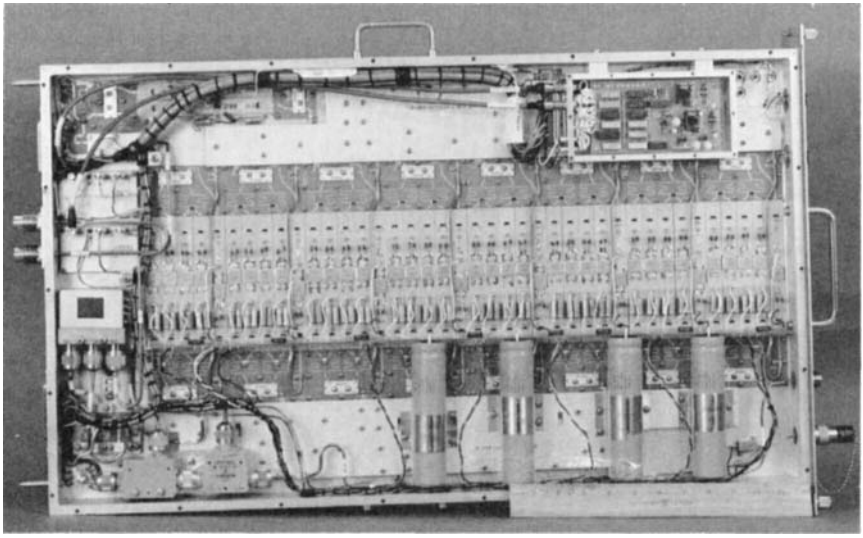


FIG. 5.19 RAMP transmitter amplifier module. (*Photograph courtesy of Raytheon Company.*)

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