18

Electronic Power Conversion

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Contents

Electronic processing of power provides the freedom to optimise the generation, conversion and use of electrical power. Most notably, it frees a system designer from the constraints of a fixed voltage supply (whether a 50/60 Hz a.c. public electricity supply or a d.c. source such as a battery). For example, wind turbines are more effective at capturing energy from the wind if freed from the constraint of rotating at synchronous speed, and pump flow rate is much more efficiently regulated through variable voltage/frequency control of the motor than through valves. But to realise the efficiency savings from varying the voltage or frequency of a power source we must ensure that the energy conversion process is itself efficient. Power electronics provides efficient means of energy conversion and has long since displaced electromechanical means.

Efficiency has been important in promoting the widespread adoption of power electronics, but the speed and degree of control that can be exercised over the power conversion process is at least as important. This control is essential in conditioning the power for an electrical machine in a machine tool or robotic manipulator. The speed of response that we can achieve from an electronic power converter depends on its implementation and, in turn, its power rating. In general, we can expect a response much faster than any electromechanical element of the system.

18.1   Electronic power conversion principles

The terms *power electronics* and *switch-mode electronics* are almost synonymous for the simple reason that semiconductors are energy efficient only when used as switches.

18.1.1   Switch-mode electronics

Voltage drop across a current carrying element is the indication of inefficiency. A transistor used in its active region (also know as the linear or amplifier region) dissipates power because it has voltage across it while carrying current. *Figure 18.1* illustrates the active region of three common devices on graphs of their output characteristics (i.e. graphs of the current through the main terminals and the voltage across those terminals for a range of controlling voltages). The three devices, the Bipolar Junction Transistor (BJT), the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and the Insulated-Gate Bipolar Transistor (IGBT) were discussed in Chapter 17.

The effect this has on system efficiency is well illustrated by two alternative ways of regulating the voltage delivered to a load. *Figure 18.2* shows a transistor used as a linear voltage regulator to reduce an input voltage, V_I down to a controlled output voltage, V_O.

As an example, consider a $5\,\Omega$ load and a regulator set to produce a 5 V output from 15 V input. The load will draw a current, I_O of 1 A. Because the current drawn from the source of the transistor is matched by current drawn in through the drain, the input current I_L will be 1 A (assuming that the control circuitry draws negligible current). The power flow will be as follows:

$$P_{out} = V_O I_O = 5\ \text{W}$$

$$P_{in} = V_I I_I \approx V_I I_O = 15\ \text{W}$$

$$P_{lost} = V_T I_O = 10\ \text{W}$$
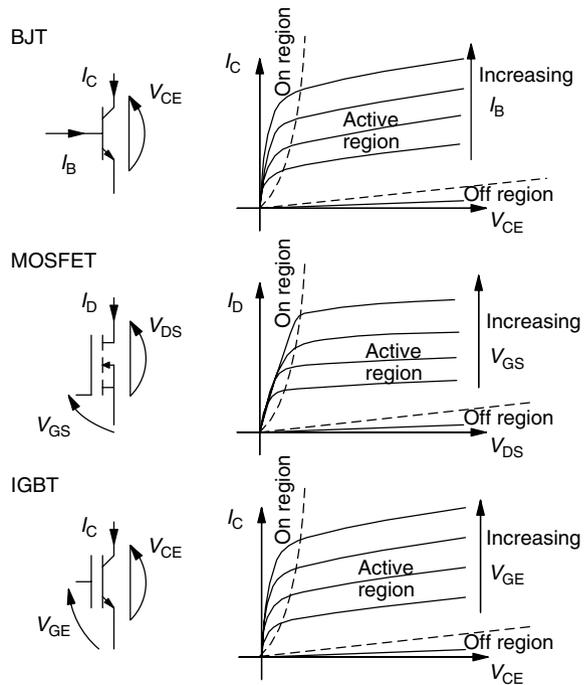
Figure 18.1   BJT, MOSFET and IGBT output characteristics and operating regions
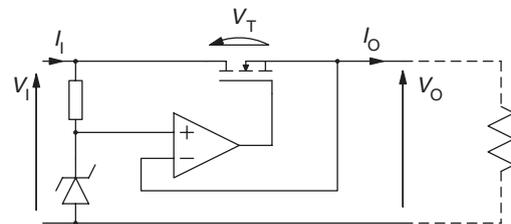
Figure 18.2   A MOSFET based linear voltage regulator

This circuit shows an efficiency of only 33%. Efficiency is important in its own right because of the need to utilise primary sources of energy well, but there is a second important reason to aim for high efficiency. The energy lost in this circuit is lost as heat in the semiconductor material. Thermal management of the semiconductor is difficult because it can be difficult to remove heat from the silicon and so its temperature will rise far above ambient. Further, the semiconductor is a small mass and its temperature will rise quickly during short periods of high dissipation. Typical maximum temperatures of silicon devices are in the range 125°–150 °C.

The alternative way of regulating the voltage across a load using a transistor is to switch the input voltage into a series of pulses. The average voltage of the pulse train is necessarily less than the input voltage. By filtering the pulse train, the ripple component of the voltage can be removed to leave only the average, that is, d.c. component to be applied to the load. *Figure 18.3* shows a transistor used to apply a pulse train to an LC filter.
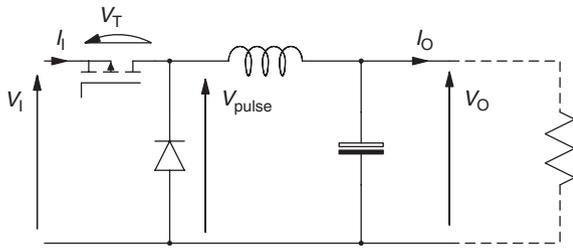
Figure 18.3   A switch-mode voltage regulator

The ratio of the on-time to the off-time can be adjusted to control the voltage delivered to the load. The output voltage will be equal to the average value of the pulse train.

$$V_O = V_{pulse}^{avg} = V_I \frac{t_{on}}{t_{on} + t_{off}} = V_I \delta \tag{18.1}$$

The ratio of the on-time to the period, δ, is known as the duty-cycle. If we wish to produce a 5 V output from a 15 V input, as we did with the linear regulator example, we would choose a duty-cycle of $\frac{1}{3}$.

Because the switch is either off (supporting voltage but not carrying current) or on (carrying current but without a voltage appearing across it) there is no coincidence of current flow and voltage drop. Therefore, there is no power dissipated in the transistor. We can also show this by considering the input and output powers. First we note that the inductor current, I_L will have the same magnitude as the output current (with no net current in the capacitor). When the switch is on, the inductor current flows as input current, I_I. When the transistor is off, the inductor current flows in the diode and no current is drawn from the input.

On state:

$$P_{out}^{on} = V_O \cdot I_O = 5\,\text{W}$$
$$P_{in}^{on} = V_I \cdot I_I = V_I \cdot I_O = 15\,\text{W}$$

Off state:

$$P_{out}^{off} = V_O \cdot I_O = 5\,\text{W}$$
$$P_{in}^{off} = V_I \cdot I_I = 0$$

On average:

$$P_{out} = V_O \cdot I_O = 5\,\text{W}$$
$$P_{in} = \frac{P_{in}^{on} \cdot t_{on} + P_{in}^{off} \cdot t_{off}}{t_{on} + t_{off}} = \frac{P_{in}^{on} \cdot t_{on}}{t_{on} + t_{off}} = P_{in}^{on} \cdot \delta = 5\,\text{W}$$

The average input power matches the output power and therefore the circuit is ideally efficient.

18.1.2   Power loss in switch-mode circuits

In principle, a switch-mode circuit can be perfectly efficient whereas a linear-mode circuit cannot. In practice, of course, there are power losses in switch-mode circuits including power loss within the semiconductors. During the off-state, a semiconductor will leak current, and therefore there will be some power dissipation. The leakage

properties of semiconductors are very good and the off-state dissipation is negligible. During the on-state, a semiconductor will drop some voltage and there will be further power dissipation. The on-state power loss is normally significant. There is also power loss as the semiconductor passes through its active region as it is switched between its on- and off-states. The average power loss is found by dividing the energy loss per cycle by the period, T. The energy loss can be expressed as an integration of the product of the instantaneous voltage and current. We can partition the cycle of switch operation into four stages: the on-state, the off-state, the turn-on transition and the turn-off transition.

$$
\begin{aligned}
P_{loss} &= \frac{1}{T} \int_0^T v_T(t) \cdot i_T(t) \cdot dt \\
&= \frac{1}{T} \left\{ \begin{array}{l} \int^{t_{on}} v_{on}(t) \cdot i_T(t) \cdot dt + \oint^{t_{off}} v_T(t) \cdot i_{off}(t) \cdot dt \\ + \int^{t_{turnon}} v_T(t) \cdot i_T(t) \cdot dt + \int^{t_{turnoff}} v_T(t) \cdot i_T(t) \cdot dt \end{array} \right\} \\
&= \frac{1}{T} \{ E_{cond} + E_{leak} + E_{turn-on} + E_{turn-off} \}
\end{aligned}
\tag{18.2}
$$

The on-state (conduction) energy loss is relatively straightforward to calculate. MOSFET devices are resistive in the on-state whereas most other devices have a near constant on-state voltage. Assuming a constant on-state voltage:

$$E_{cond} = V_{on} \cdot I_{on}^{avg} \cdot t_{on} \tag{18.3}$$

Calculation of switching power loss requires detailed knowledge of the trajectory taken through the active region. This is dependent on the gate drive arrangement and the circuit topology.[6] *Figure 18.4* illustrates a simple case where the load is inductive (and treated as a constant current element, I_L) and is switched from a supply voltage of V_S. Diode recovery has been ignored and the transistor has been assumed to operate as a controlled current source while in its active region. The switching trajectory of MOSFETs and IGBTs and the reverse-recovery characteristics of diodes were discussed further in Chapter 17 (Sections 17.5, 15.6 and 17.1.2).

(I)   During the off-state, the load current flows in a loop involving the diode, and the transistor must support the full supply voltage (plus diode forward voltage drop).

(II)   At turn-on, the transistor begins to take current from the load and this current is assumed to rise linearly. The portion of load current not taken by the transistor continues to flow in the diode. Therefore, the diode is held in forward bias and the full supply voltage still appears across the transistor. Once the transistor current has risen to equal the load current, the diode ceases to conduct. (It is at this point that reverse-recovery will occur in a real diode as discussed in Section 17.2.1). The transistor voltage falls as the parasitic capacitances (of the diode and transistor) charge/discharge and the diode becomes reverse biased. The figure is drawn assuming the change of voltage is also linear.
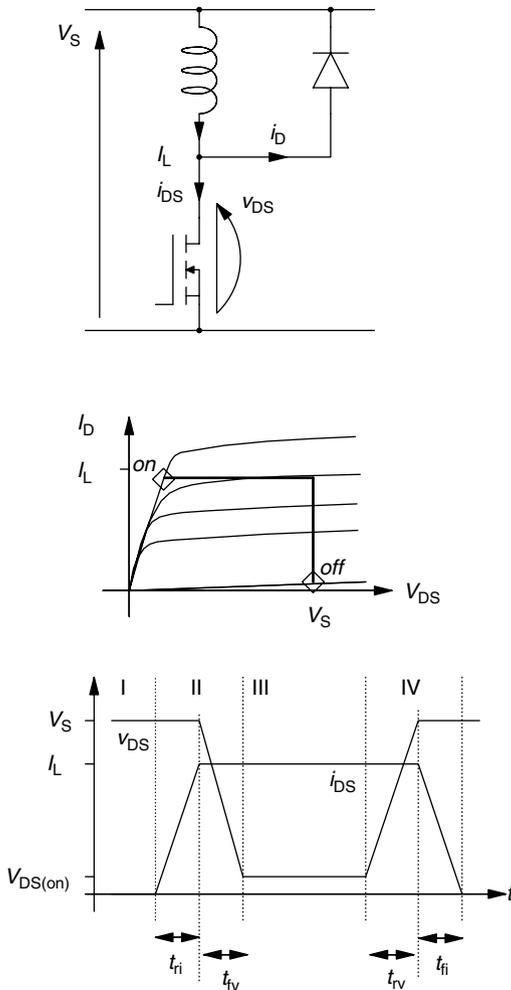
Figure 18.4 A MOSFET switching an inductive load, its trajectory through output characteristic and its drain current and drain-source voltage waveforms

(III) During the on-state, the load current flows in the transistor.
(IV) When turn-off of the transistor is initiated, the decrease of current flow through the transistor diverts current into the parasitic capacitances of the transistor and diode. The voltage across the transistor rises as a result of this. The voltage rises until it exceeds the supply voltage and the diode is forced into conduction. Once the diode is conducting, the transistor current can fall and the load current diverts into the diode.

With the assumptions of linear rise and fall of both voltage and current, the turn-on and turn-off energy loss can be found:

$$E_{\text{turn-on}} = \tfrac{1}{2} V_S I_L (t_{\text{ri}} + t_{\text{fv}})$$
$$E_{\text{turn-off}} = \tfrac{1}{2} V_S I_L (t_{\text{rv}} + t_{\text{fi}}) \Leftarrow \qquad (18.4) \Leftarrow$$

Some devices, notably MOSFETs, are specified in terms of the rise and fall times during switching (under standard conditions). Others, notably IGBTs, that have more complex switching transients are specified in terms of the energy loss during switching (again, for standard conditions).

It is normal to express the loss in terms of power rather than energy and so we divide the energy loss per cycle by the period of the cycle.

$$
\begin{aligned}
P_{\text{loss}} &= \frac{1}{T} \left(E_{\text{cond}} + E_{\text{turn-on}} + E_{\text{turn-off}} \right) \Leftarrow \\
&= \delta \varsigma\, V_{\text{on}} \cdot I_{\text{on(avg)}} + f \cdot \left(E_{\text{turn-on}} + E_{\text{turn-off}} \right) \Leftarrow \\
&= Conduction\ loss + Switching\ loss
\end{aligned}
\qquad (18.5)
$$

The power loss due to leakage in the off state has been neglected.

It is important to note that because the switching loss is an energy loss per operation, the power loss is proportional to switching frequency, f; whereas the conduction loss is simply an average power loss as indicated by the duty cycle, δ. The dependence of power loss on frequency acts against the desire to increase switching frequency that would otherwise bring benefits of faster response and the opportunity to use smaller passive components.

Proper thermal design of a power electronic system is essential to its success. There needs to be management of the power loss through operating mode or circuit design. Choice can be exercised over the package style for its heat transfer properties. The heat-sink to which the semiconductors are attached is often a bulky and expensive part of the system. Its type (natural convection, forced-air, liquid-cooled) and rating (temperature rise per unit power loss) must be carefully chosen.[6]

18.2 Switch-mode power supplies

There is a large variety of circuits available for converting power at one d.c. voltage to another. The linear regulator, introduced in *Figure 18.2*, offers only a step-down of voltage. Switch-mode power supplies, SMPS, can offer step-down, step-up and negation of the voltage through the three basic circuit topologies, *viz.*, Buck, Boost and Flyback. Three further topologies, *viz.*, Čuk, SEPIC and Zeta, add extra passive components in order to improve secondary aspects such as current and voltage ripple. A family of circuits has been derived from the basic family that incorporate mutually coupled inductors to offer galvanic isolation between input and output. Another family of circuits, to be discussed in, Section 18.6 has been developed that incorporate a resonant element so that the switching trajectory of the transistor is modified to reduce power loss and enable higher frequency operation. The sections that follow cover a selection of the many circuits that are described in the literature. A fuller description and a wider selection of circuits are to be found.[2,3,6] Here, the description of the Buck SMPS is used to introduce several of the basic principles of analysis that apply to all SMPS circuits.

18.2.1 Buck SMPS

The Buck circuit has already been introduced in *Figure 18.3* as the direct competitor to the linear regulator. Its operating principle is the storage and release of energy in the inductor during its two states as illustrated in *Figure 18.5*.
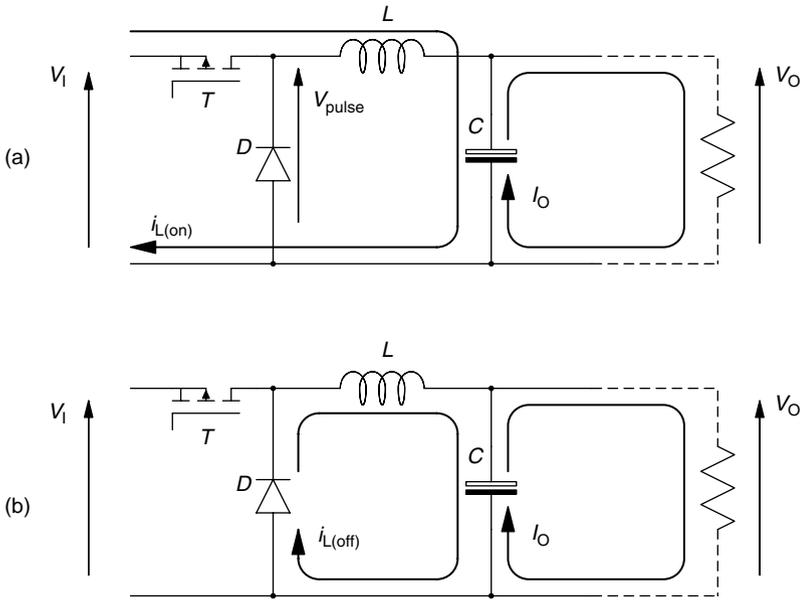
Figure 18.5   Current paths in the on- and off-states of a Buck SMPS

The operation of the circuit can be summarised as:

On-state (*Figure 18.5(a)*):
- A voltage is imposed across the inductor of:

$$V_L = V_I - V_{DS(on)} - V_O$$

$$\approx V_I - V_O$$

- The current in the inductor increases according to:

$$\frac{di_L}{dt} = \frac{V_I - V_O}{L}$$

- The energy stored in the inductor increases.
- Energy is also delivered to the output.

Off-state (*Figure 18.5(b)*):
- The current flow through the inductor is maintained by its stored energy.
- The diode is forced into conduction to provide path for the current.
- A voltage is imposed across the inductor of:

$$V_L = -V_{DS(on)} - V_O$$

$$\approx -V_O$$

- The current in the inductor decreases according to:

$$\frac{di_L}{dt} = \frac{V_I - V_O}{L}$$

- The energy stored in the inductor decreases.
- Energy continues to be delivered to output.

This analysis shows that the inductor current ripples up and down. The circuit will settle into a periodic steady-state condition such that the inductor current at the end of the cycle is the same value as at the beginning. The capacitor is chosen to be sufficiently large that the voltage across it changes very little during the cycle. It too will have ripple, and again the voltage at the end of the cycle will match that at the beginning.

There are two cases to examine. The first is known as continuous conduction and is the case where the decrease of current does not take it to zero. *Figure 18.6(a)* illustrates the principal voltage and current waveforms. The second case is known as discontinuous conduction and is where the decrease of current does take it to zero and the inductor has released all of its stored energy. The current will remain at zero until the switch is next turned on *Figure 18.6(b)*.

Applying Kirchhoff's current law to the node at the output, we can state that for every instance in time:

$$i_L = i_C + i_O$$

If we assume that the output current is constant (because the output voltage is very nearly so) we can write $i_O = I_O$. Then taking the average current:

$$i_L^{avg} = i_C^{avg} + I_O$$

In periodic steady-state there can be no average current flow through the capacitor. We can consider the inductor current to be composed of a constant component that flows through the load and a ripple component that diverts through the capacitor.

A relationship between the output voltage and the switching of the transistor follows from the statement that there is no net change in inductor current over a cycle. That is, the increase in current during the on-time of the transistor is matched by the decrease of current when the current flows in the diode. Here we make a distinction between the diode conduction time and the off-time because in the case of discontinuous conduction the diode does not conduct for all of the off-time.
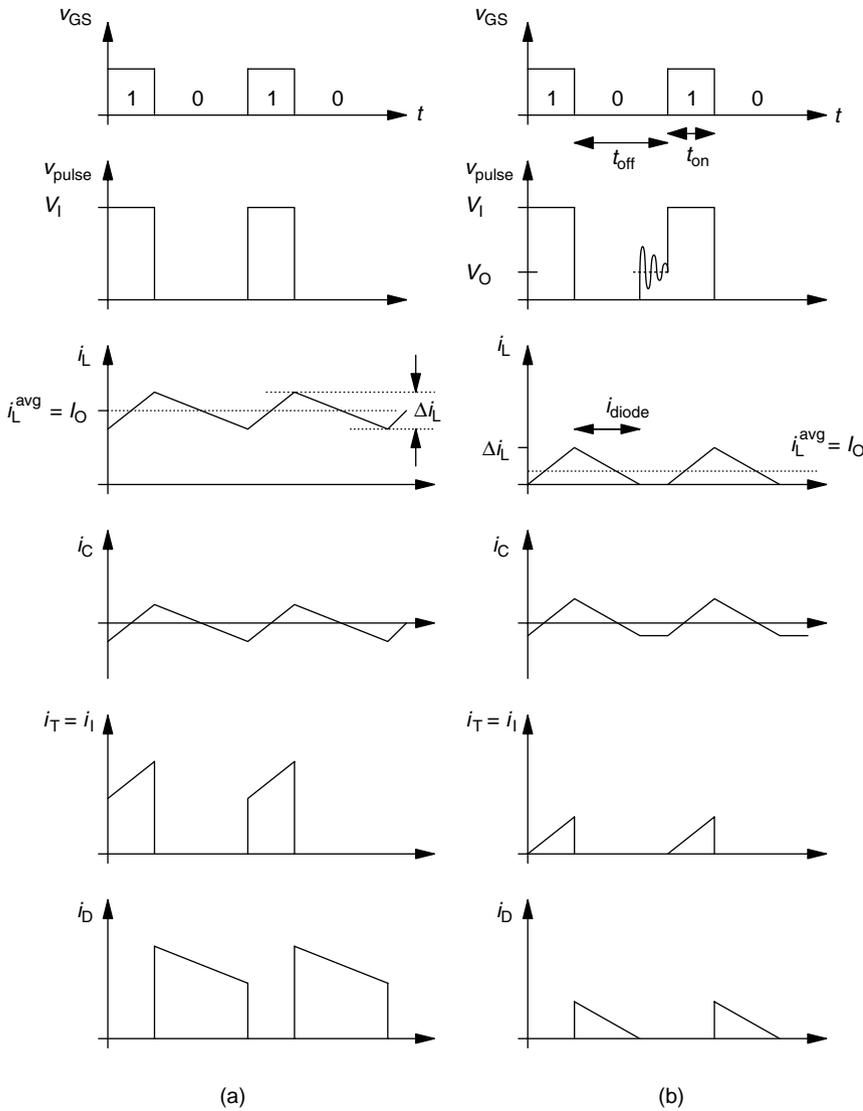
Figure 18.6   Voltage and current waveforms of the Buck SMPS in *Figure 18.5* for (a) continuous and (b) discontinuous inductor current

$$\Delta i_{L(on)} + \Delta i_{L(diode)} = 0$$

$$\Delta i_{L(on)} = \frac{di_L}{dt} t_{on} = \frac{V_I - V_O}{L} t_{on} \qquad (18.6)$$

$$\Delta i_{L(diode)} = \frac{di_L}{dt} t_{diode} = \frac{-V_O}{L} t_{diode}$$

$$\frac{V_O}{V_I} = \frac{t_{on}}{t_{on} + t_{diode}} \qquad (18.7)$$

For the continuous conduction case, $t_{diode} = T_{off}$ and the output/input ratio is simply the duty-cycle of the switch, δ.

$$\frac{V_O}{V_I} = \delta \qquad (18.8)$$

This is a very convenient relationship. It means that the output voltage is a linear function of the duty-cycle of the switch, as shown in *Figure 18.7*. This is something we can set easily and accurately. However, if the circuit operates in discontinuous mode the relationship is more complex. The conduction becomes discontinuous if the average inductor current (and therefore the output current) becomes small in comparison to the ripple. It is the magnitude of output current that dictates the proportion of the off-time for which the diode conducts. The output current in discontinuous mode is calculated by taking the average of the inductor current illustrated in *Figure 18.6(b)*.

$$I_O = i_L^{avg} = \frac{1}{T} \int_0^T i_L \cdot dt = \frac{\frac{1}{2}(t_{on} + t_{diode}) \cdot \Delta i_L}{T} \qquad (18.9)$$
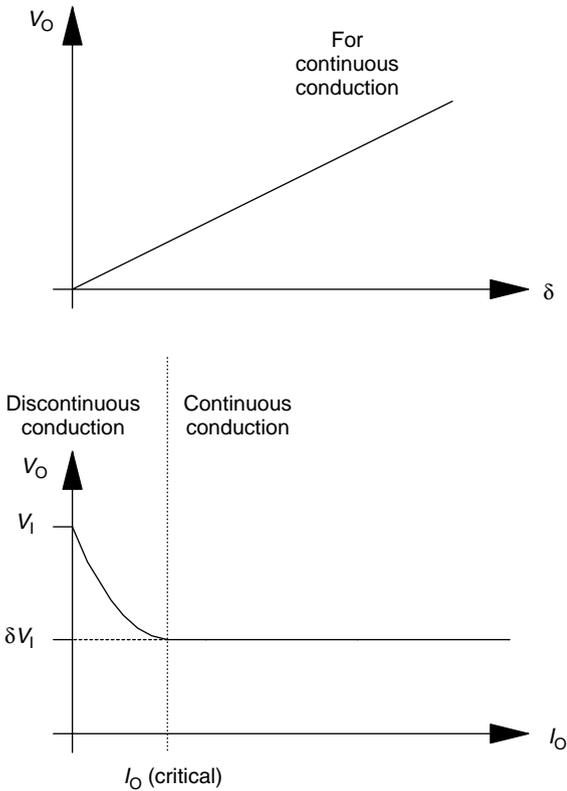
Figure 18.7 Output voltage as a function of duty-cycle and output current

Substituting Equations 18.6 and 18.9 into Equation 18.7 and using the relation $f = 1/T$ yields:

$$\frac{V_O}{V_I} = \frac{1}{1 + \frac{2I_O \ Lf}{V_I \ \delta^2}}$$
(18.10)

Figure 18.7 also shows a typical graph of output voltage of a buck converter operated at constant duty-cycle as the output current is increased. There are two regions: discontinuous and continuous operation. The critical conduction point is when $I_O = \frac{1}{2}\Delta i_L$. At currents higher than this, the output voltage is constant, as predicted by Equation 18.8. In practice, the voltage will decrease slightly with current because of voltage drops across the semiconductors and the resistance of the inductor. Below the critical current, the voltage rises with decreasing current, according to Equation 18.10 until reaching the input voltage at zero output current.

The switching action of the transistor leads to voltage ripple on the output capacitor. This ripple may interfere with the operation of the circuit being supplied at the output. It is important to analyse this ripple and make design choices that reduce it. The capacitor current waveform was shown in *Figure 18.6*. The ripple voltage developed across the capacitor can be found by integrating this current.

$$v_C = \frac{1}{C}\int i_C \cdot dt$$
(18.11)

Since the ripple must be centred on zero to have an average value of zero, we can find the ripple amplitude from the area under the positive excursion of the current (i.e. the charge delivered to the capacitor while the inductor current exceeds the load current). For continuous conduction the ripple is:

$$\Delta v_C = \frac{1}{8fC\Delta i_L}$$
(18.12)

Using typical values of switching frequency and current ripple it becomes clear that capacitors of the order of $100\,\mu F$ are sufficient to keep the voltage ripple in the order of $10\,mV$. However, this is a misleading calculation because the parasitic components of the capacitor make a significant, in fact a dominant, contribution to the ripple voltage. *Figure 18.8* shows the form (but not relative magnitude) of the ripple contributions. Another consideration is that much larger capacitors than indicated by Equation 18.12 are often used for providing some energy storage for supply-loss ride-through.

The magnitude of the voltage ripple due to the Effective Series Resistance, ESR is given by:

$$\Delta v_{ESR} = R_{ESR} \ \Delta i_L$$
(18.13)

The magnitude of the voltage ripple due to the Effective Series Inductance, ESL, is given by:

$$\Delta v_{ESL} = L_{ESL} \ \Delta i_L \left(\frac{1}{t_{on}} + \frac{1}{t_{off}}\right) = L_{ESL} \ \Delta i_L \ f \frac{1}{\delta(1-\delta)}$$
(18.14)

So, for a given current ripple, the voltage ripple due to the capacitance is inversely proportional to frequency and is normally insignificant. The voltage ripple due to the ESR is independent of frequency and is significant. The voltage ripple due to the ESL is proportional to frequency and is
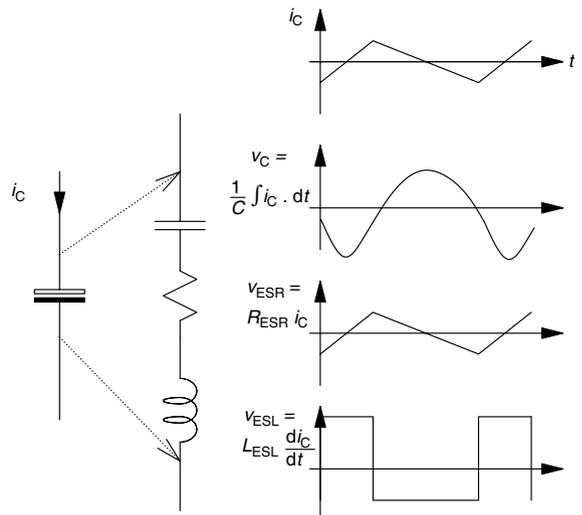
Figure 18.8 Contribution to ripple voltage from the effective series resistance (ESR) and inductance (ESL) of a capacitor

significant. In other words, the output capacitor is chosen for its ESR and ESL properties and its capacitance is normally satisfactory by default.

The output capacitance is not the only component for which parasitic effects are observed. *Figure 18.6(b)* illustrates a parasitic oscillation of V_{pulse}, the voltage across the diode, as the diode falls out of conduction when the inductor current reaches zero. In an ideal circuit we would expect V_{pulse} to rise to V_O so that no voltage appears across the inductor. In practice, this requires the junction capacitance of the diode to charge via the inductor as the diode enters reverse bias. Thus, a second order system is formed and a lightly damped oscillation of the voltage occurs.

18.2.1.1 Two and four quadrant chopper

The Buck SMPS is used at power ratings of less than 1 W to more than 1 MW. The larger versions are generally for control of d.c. machines in drive systems as discussed in Chapter 19 (Section 19.3.3.2, 'Step-down d.c.–d.c. converters'). The load is the armature circuit of the machine. The filtering action at the output is often inherent in the inductance of the armature winding and the inertia of the mechanical system (that keeps the speed and back-EMF constant over the short term). In some cases, extra inductance will be added to keep the current ripple low and prevent either excessive power loss in the armature resistance or torque ripple.

The simple chopper of *Figure 18.9(a)* is limited as a motor drive. The output voltage can only be varied between 0 and V_s. In particular, the voltage cannot be made negative and, therefore, reverse rotation cannot be supported. Further, there is no path for reverse armature current so it is not possible to develop reverse torque to decelerate the mechanical system (through regeneration). This circuit is known as a one-quadrant chopper because it can operate the drive only in the first quadrant of the torque–speed plane, *Figure 18.10*.

The circuit of *Figure 18.9(b)* allows controlled negative current. The switches are operated in anti-phase, i.e. T_1 is on for period δT and T_2 for period $(1-\delta)T$. This forces the voltage V_A to become a pulse train of amplitude V_S and duty-cycle δ regardless of the direction of I_A. If the direction of I_A is such that it cannot flow in the switch that is on, then it will flow in the anti-parallel diode. The circuit is still constrained to positive voltage. It can therefore operate a drive in the first and fourth quadrants.

(a)

(b)

(c)
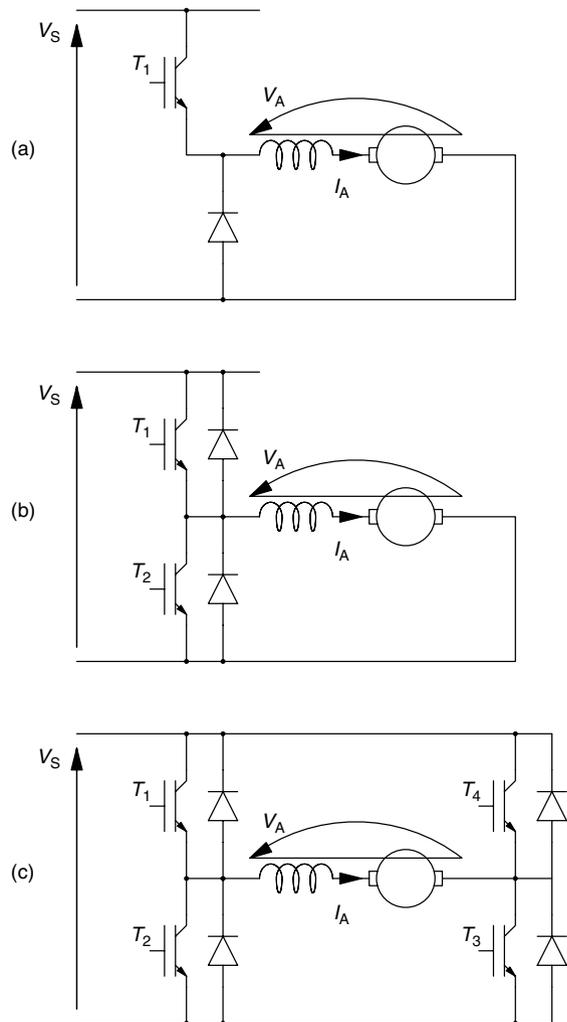
Figure 18.9 One, two and four quadrant choppers
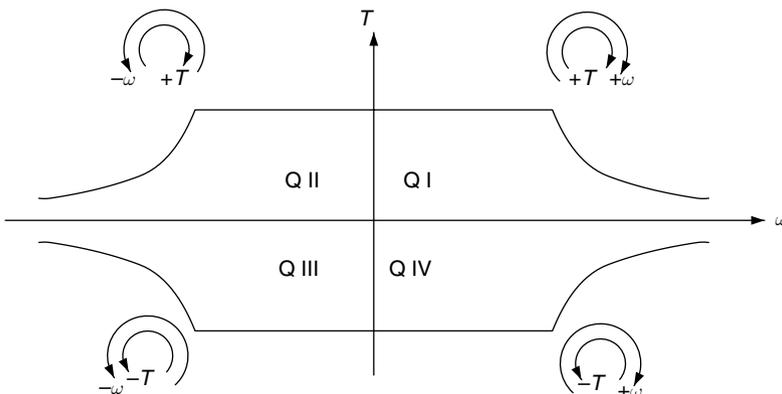
Figure 18.10 Quadrants of the torque–speed plane

The circuit of *Figure 18.9(c)* is variously known as a four-quadrant chopper, a full bridge or an *H*-bridge. There are several ways to operate the circuit. The transistor pair T_1 and T_2 can be operated in anti-phase as in the two-quadrant chopper. Then T_3 can be switched with T_1 and T_4 switched with T_2. Alternatively, T_3 and T_4 are not switched but simply used to select the polarity of the voltage. The circuit allows both directions of current flow and both polarities of output voltage. Therefore, the drive can be operated in all four quadrants.

18.2.2   Boost SMPS

The Boost circuit is a simple re-arrangement of the components of the Buck circuit, *Figure 18.11*.

As in the case of the Buck SMPS, energy storage in the inductor is the key to its operation. If the switch were left off for a long time, then the output capacitor would charge up via the inductor and diode to a voltage equal to the input voltage. The switching action then raises the output voltage above the input voltage hence the name Boost.

Operation of the circuit can be summarised as:

On-state (*Figure 18.12(a)*):
- The input voltage is imposed across the inductor:

$$V_L = V_I - V_{DS(on)} \Leftarrow$$
$$\approx V_I$$

- The current in the inductor increases as:

$$\frac{di_L}{dt} = \frac{V_I}{L} \Leftarrow$$

- The energy stored in the inductor increases.
- The diode is reverse biased and the load is supplied by the capacitor alone.

Off-state (*Figure 18.12(b)*):
- The current flow through the inductor is maintained by its stored energy.
- The diode is forced into conduction to provide a current path.
- A voltage is imposed across the inductor of:

$$V_L = V_I - V_{D(on)} - V_O$$
$$\approx V_I - V_O$$

- The current in the inductor decreases because the output voltage is higher than the input voltage:

$$\frac{di_L}{dt} = \frac{V_I - V_O}{L} \Leftarrow$$

The energy stored in the inductor decreases as it is transferred to the capacitor and output.

The inductor current ripples up and down, and again there are two cases to examine. If the average current is large then the inductor will be in continuous conduction, *Figure 18.13(a)*. If the average current is small then the inductor will be in discontinuous conduction, *Figure 18.13(b)*.

Again following the principle that in steady-state the change in inductor current during the on-state must be matched by the change during the off-state, we can derive a relationship between input voltage, output voltage and the timing of the switch operation.

$$\Delta i_{L(on)} + \Delta i_{L(diode)} = 0$$

$$\Delta i_{L(on)} = \frac{di_L}{dt} t_{on} = \frac{V_I}{L} t_{on} \qquad (18.15) \Leftarrow$$

$$\Delta i_{L(diode)} = \frac{di_L}{dt} t_{diode} = \frac{V_I - V_O}{L} t_{diode}$$

$$\frac{V_O}{V_I} = \frac{t_{on} + t_{diode}}{t_{diode}} \qquad (18.16) \Leftarrow$$

For the continuous conduction case where $t_{diode} = t_{off}$ the output/input relationship is a simple, but non-linear, function of δ.

$$\frac{V_O}{V_I} = \frac{1}{1 - \delta_\varsigma} \qquad (18.17) \Leftarrow$$

For the discontinuous case, the relationship again becomes dependent on the circuit conditions. The relationship is found by expressing the average inductor current (equal to the input current) in terms of the diode conduction time.

$$\frac{V_O}{V_I} = \frac{1}{1 - \frac{V_I \delta^2}{2I_I Lf}} \qquad (18.18) \Leftarrow$$

It is important to note that the Boost circuit suffers a disadvantage in terms of the output voltage ripple. This is because the capacitor and output are supplied only when
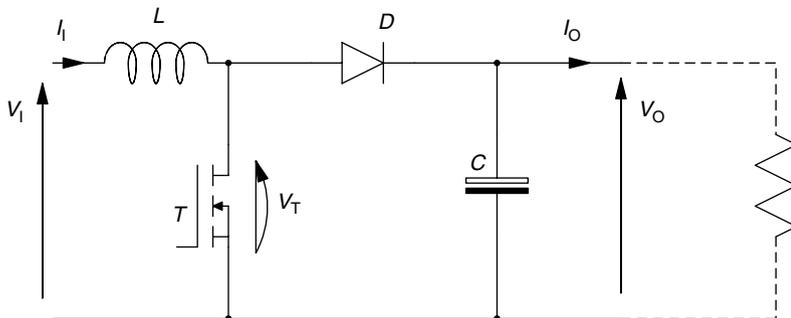
Figure 18.11   The Boost SMPS
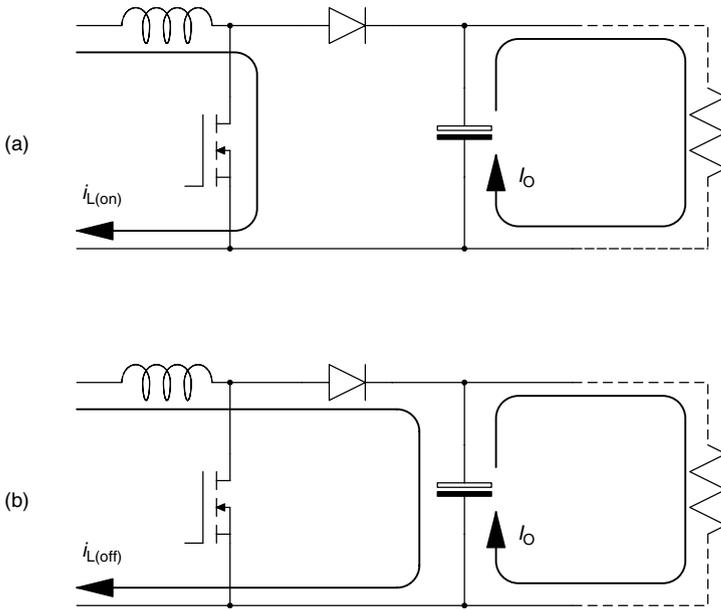
Figure 18.12 Current paths in on- and off-states of the Boost SMPS

the diode conducts, whereas in the Buck they are continually supplied via the inductor (provided that the inductor is in continuous conduction). The average component of the diode current flows onward to the load, and the ripple component flows in the capacitor. As can be seen from *Figure 18.13*, the ripple component of the diode current is larger than the ripple of the inductor current and is, in fact, at least as large as the output current.

On the other hand, the Boost SMPS draws an essentially smooth input current whereas the Buck SMPS draws a pulsed input current. This may be important if the interference generated in the input line is an issue.

18.2.3   Flyback SMPS

The Flyback SMPS is another rearrangement of the basic components as shown in *Figure 18.14*. This circuit is also known as the Buck-Boost SMPS. Some texts, such as,[3] reserve the name Flyback for the transformer isolated version of the circuit to be described in Section 18.2.5.

Operation of the circuit is as follows: the transistor is switched on to impose the input voltage across the inductor and store energy in that inductance. *Figure 18.15* shows the current paths in on- and off-states. It is clear that the release of the inductor energy by current flow through the diode charges the capacitor such that its lower plate becomes the more positive. In other words, the output voltage is negative.

The negation of the voltage is also apparent from the transfer characteristic which is derived from the assumption of steady-state in the normal way:

$$\Delta i_{L(on)} + \Delta i_{L(diode)} = 0$$

$$\Delta i_{L(on)} = \overleftarrow{\frac{di_L}{dt}} t_{on} = \overleftarrow{\frac{V_I}{L}} t_{on} \qquad (18.19)\Leftarrow$$

$$\Delta i_{L(diode)} = \overleftarrow{\frac{di_L}{dt}} t_{diode} = \overleftarrow{\frac{V_O}{L}} t_{diode}$$

$$\frac{V_O}{V_I} = -\frac{\overleftarrow{t_{on}}}{t_{diode}} \qquad (18.20)\Leftarrow$$

If the circuit is in continuous conduction, the transfer characteristic becomes:

$$\frac{V_O}{V_I} = -\frac{\overleftarrow{\delta\varsigma}}{1 - \delta\varsigma} \qquad (18.21)\Leftarrow$$

Thus, the circuit is capable of step-down (for $\delta < 1/2$) or step-up (for $\delta > 1/2$) but with a voltage negation as well.

For discontinuous conduction the transfer characteristic is:

$$\frac{V_O}{V_I} = -\frac{V_O\delta^2}{2\overleftarrow{I_{I(avg)}}Lf} \qquad (18.22)\Leftarrow$$

The principal current and voltage waveforms in continuous and discontinuous conduction are shown in *Figure 18.16*. It can be seen that both the input current and the capacitor current are pulsed waveforms and, as a consequence, there can be large current ripple at both the input and output.

18.2.4   Capacitor coupled SMPS

A new family of SMPS can be formed by adding an extra capacitor and an extra inductor to the basic elements, *Figure 18.17*. The capacitor is part of the energy transfer process and is (partially) charged and discharged during the cycle of operation. They have voltage transfer relationships similar to that of the Flyback (with or without the negation) and are therefore capable of step-up or step-down depending on the duty-cycle. The Ćuk SMPS, *Figure 18.17(a)*, (named after its inventor) provides an identical transfer characteristic to the Flyback SMPS but has inductors in both the input connection and the charging path of the
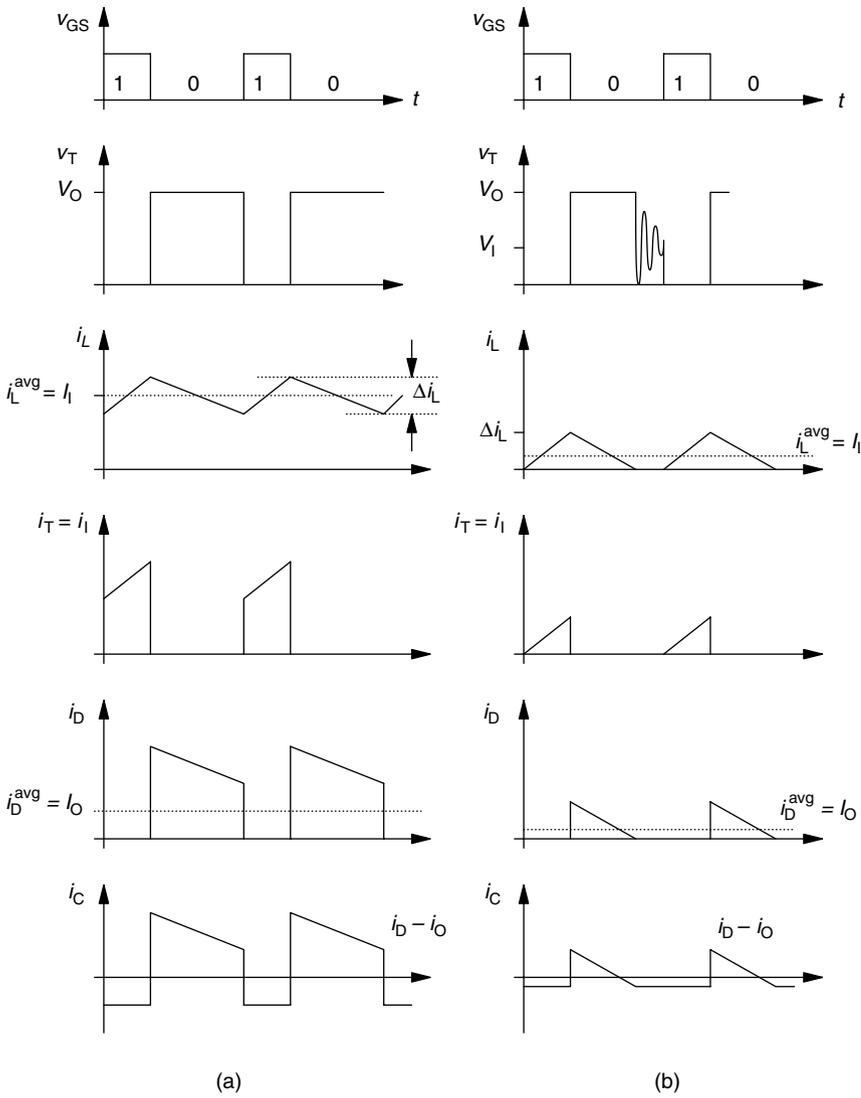
Figure 18.13   Voltage and current waveforms of the Boost SMPS for (a) continuous and (b) discontinuous inductor current
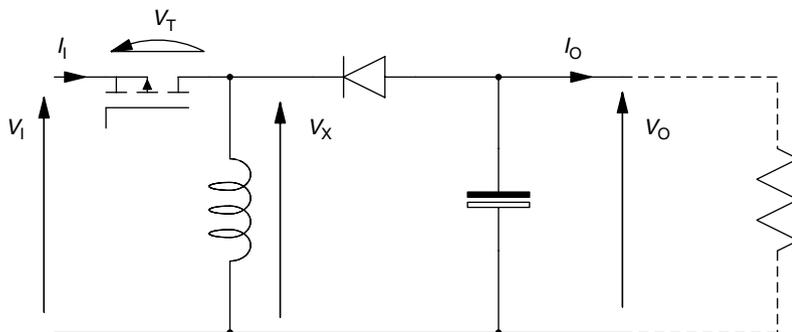
Figure 18.14   The Flyback SMPS
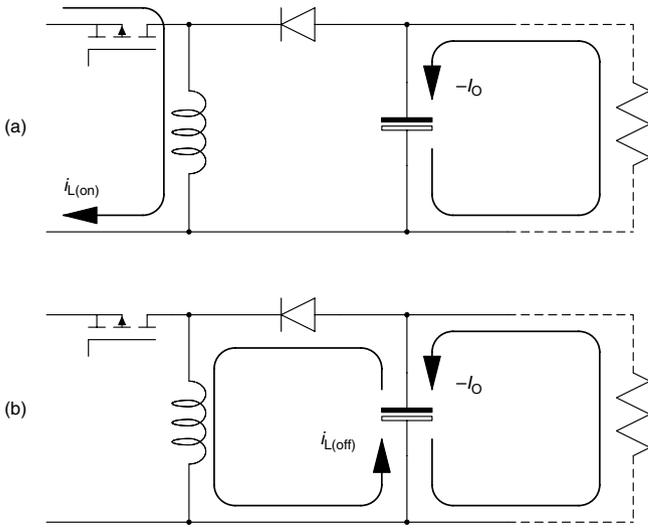
Figure 18.15 Current paths in on- and off-states of the Flyback SMPS
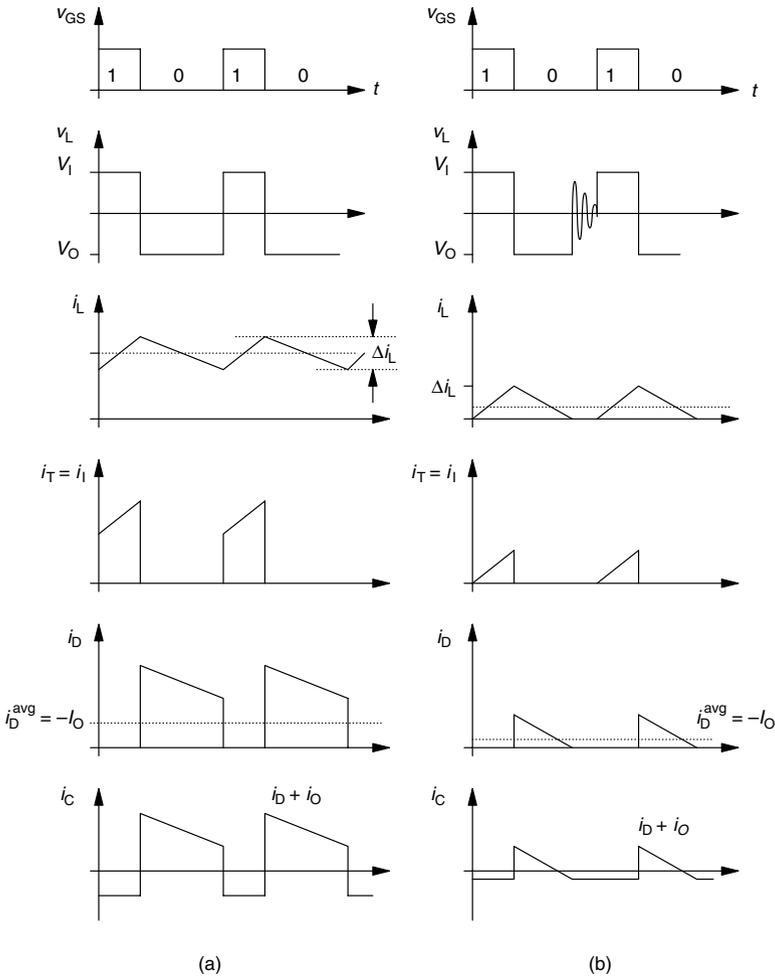
Figure 18.16 Voltage and current waveforms of the Flyback SMPS for (a) continuous and (b) discontinuous inductor current
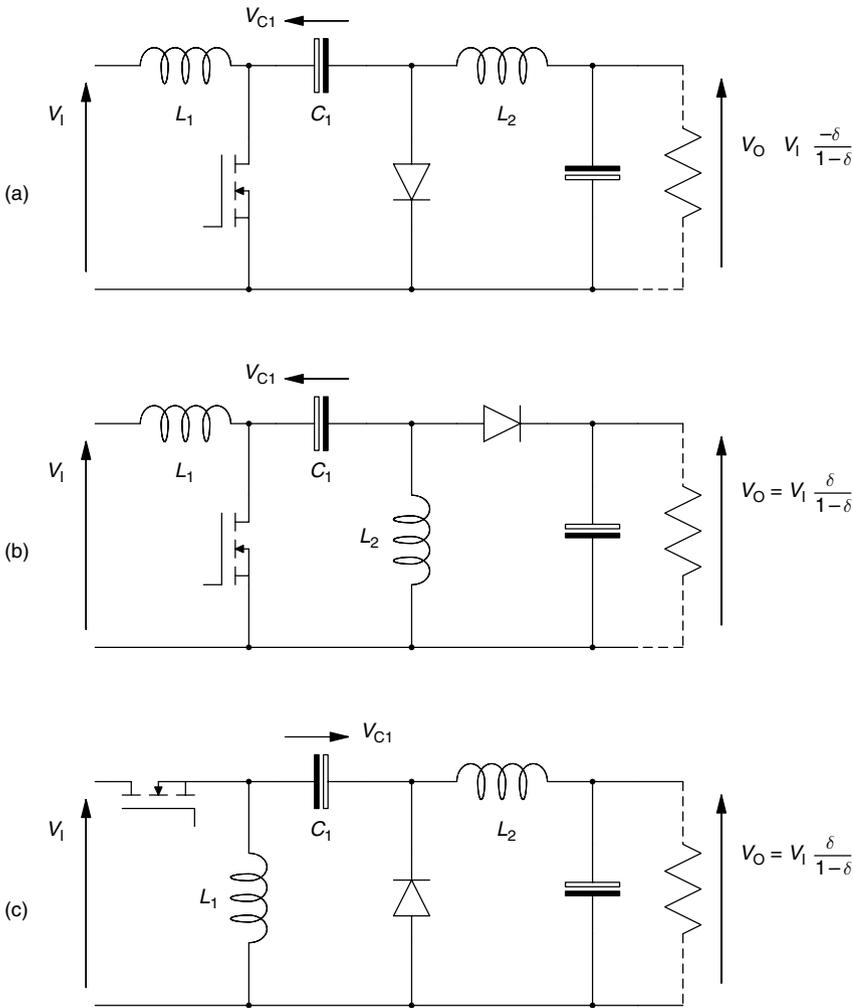
Figure 18.17 Čuk, SEPIC and Zeta SMPS

output capacitor. This provides low input current ripple and low output voltage ripple[3]. The SEPIC SMPS, *Figure 18.17(b)*, (single-ended primary inductor converter) and Zeta SMPS, *Figure 18.17(c)*, have an non-inverted output voltage and are capable of step-up or step-down. These two circuits differ in whether the input or output current is smoothed by an inductor.

18.2.5 Isolated flyback SMPS

Energy storage in the inductor is the key to SMPS operation. Energy can be built up by imposing one voltage and released into another. The energy is stored temporarily in the magnetic field of the inductor. If we use mutually coupled inductors then we can go one step further. We can build up stored energy in the magnetic field using one circuit and release the energy using an entirely separate circuit. Thus, we can achieve galvanic isolation between the input and output. This is useful for transferring energy from a ground-referenced supply to a non ground-referenced supply.

Figure 18.18 shows a Flyback SMPS incorporating a mutually coupled pair of inductors such that the input and output circuits do not have any direct electrical connection.

The current paths illustrated in *Figure 18.19* are very similar to those of the non-isolated Flyback circuit, *Figure 18.15*.

In analysing the operation of the circuit, it is helpful to discuss the flux, ϕ in the inductor core rather than the current. These two quantities are closely related, Equation 18.23 (which is written to include the possibility of more than two coupled inductors), but flux is the more useful quantity because it more directly relates to the stored energy in the magnetic field and is the quantity that must remain continuous from instant to instant (i.e. have a finite derivative).

$$\phi = \frac{N_1}{\mathcal{R}} i_1 + \frac{N_2}{\mathcal{R}} i_2 + \cdots$$

or

$$\phi = \frac{L_1}{N_1} i_1 + \frac{L_2}{N_2} i_2 + \cdots \tag{18.23}$$
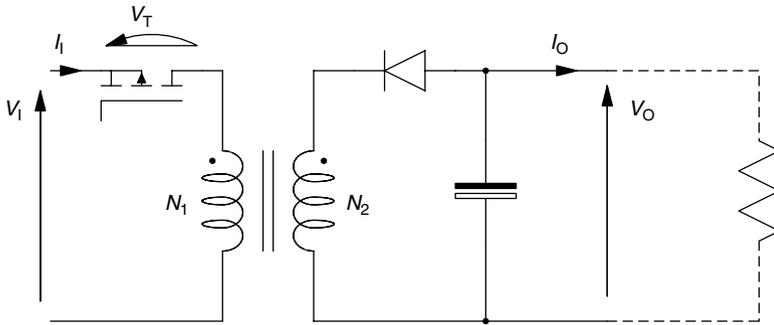
Figure 18.18   An isolated Flyback SMPS using a mutually coupled pair of inductors

where N is the number of turns of a winding, L is its inductance and $\mathscr{R}$ is the reluctance of the magnetic path.

The voltage induced across any of the mutually coupled inductors is given by Faraday's Law and for the first inductor is expressed as:

$$E_1 = N_1 \frac{d\phi}{dt}$$
$$= \frac{N_1^2}{\mathscr{R}} \frac{di_1}{dt} + \frac{N_1 N_2}{\mathscr{R}} \frac{di_2}{dt} + \cdots \qquad (18.24)$$

or

$$= L_1 \frac{di_1}{dt} + M_{12} \frac{di_2}{dt} + \cdots$$

With these relations in mind, we can draw the principal voltage and current waveforms as shown in *Figure 18.19*. There are two cases: continuous conduction (defined as the flux in the core not reaching zero by the end of the cycle) and discontinuous conduction (defined as flux reaching and holding zero by the end of the cycle). The flux rises linearly

while the transistor is on because of the voltage imposed across the primary. When the transistor switches off, the primary current must stop and the diode is forced into conduction so that secondary current can flow to maintain the flux. The primary and secondary side currents are scaled versions of the flux according to the number of turns. When the diode is conducting, a voltage is imposed across the secondary and this is reflected on the primary according to the turns-ratio. Thus, the transistor must support $V_I + V_O\, N_1/N_2$ while it is off.

The transfer characteristic can be evaluated from rise and fall of flux in steady-state.

$$\Delta\phi_{(on)} + \Delta\phi_{(diode)} = 0$$
$$\Delta\phi_{(on)} = \frac{d\phi}{dt} t_{on} = \frac{V_I}{N_1} t_{on}$$
$$\Delta\phi_{(diode)} = \frac{d\phi}{dt} t_{diode} = \frac{V_O}{N_2} t_{diode}$$
$$\frac{V_O}{V_I} = -\frac{N_2}{N_1} \frac{t_{on}}{t_{diode}} \qquad (18.25)$$
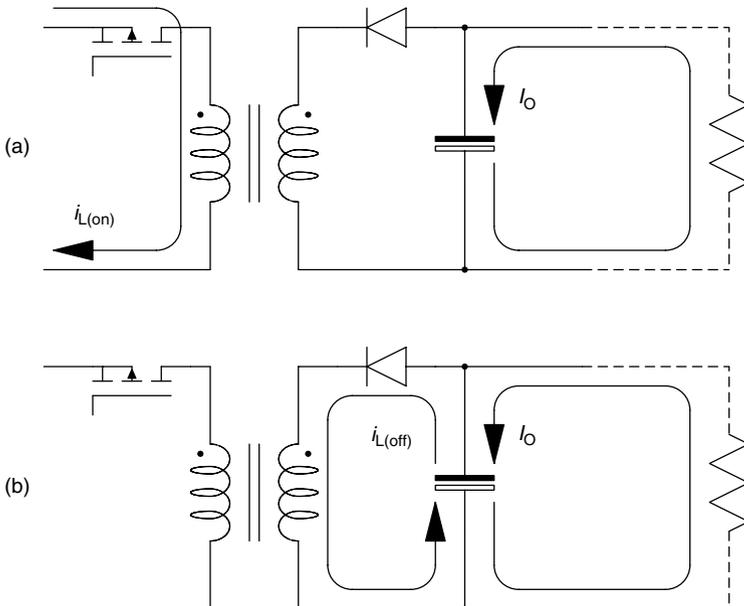
Figure 18.19   Current paths in on- and off-states of the isolated Flyback SMPS

Because the output is isolated, we can choose to take the output voltage in either sense and it is more normal to see the circuit drawn as in *Figure 18.21*. In this circuit the primary has also been rearranged to give a ground referenced MOSFET connection. The transfer characteristic for continuous conduction is:

$$\frac{V_O}{V_I} = \frac{N_2}{N_1}\frac{\delta\varsigma}{1-\delta\varsigma} \qquad (18.26)\Leftarrow$$

Discontinuous operation is sometimes favoured because it is easy to ensure that the core does not saturate. It is quite useful from a control standpoint because a fixed amount of energy is delivered to the output in each cycle.

The waveforms of *Figure 18.20* were drawn assuming perfect coupling of the flux to each winding. In practice, this will not be the case and each winding will have a leakage field. The consequence of this is that the currents in the primary and secondary cannot rise and fall instantaneously. In particular, when the transistor is switched off the primary current will not cease until the energy in the primary leakage field has been removed. The current will overcharge the parasitic capacitance of the transistor, as illustrated in *Figure 18.22*.

The overshoot can be estimated by assuming that all of the energy previously stored in the leakage field is transferred to the drain-source capacitance. The voltage overshoot has important implications for the rating of the transistor. Using a resistor-capacitor-diode snubber can reduce the over-voltage[6] but power loss in the snubber is problematic and it is difficult to design it for a wide range of operating currents. More sophisticated clamp-like snubbers are difficult to apply because of the lack of a suitable voltage rail to which to clamp.

The transistor over-voltage problem can be solved, at the expense of another transistor, by switching both ends of the primary winding as shown in *Figure 18.23*. Each transistor can be rated for V_I rather than $V_I + V_O N_1/N_2 + V_{overshoot}$ which would be required for the single transistor. The energy stored in the leakage field of the primary is returned to the supply via the two diodes. It is important that these diodes do not conduct in place of the output-side diode during normal operation and so the reflected secondary voltage $V_O N_1/N_2$ must be kept less than V_I.
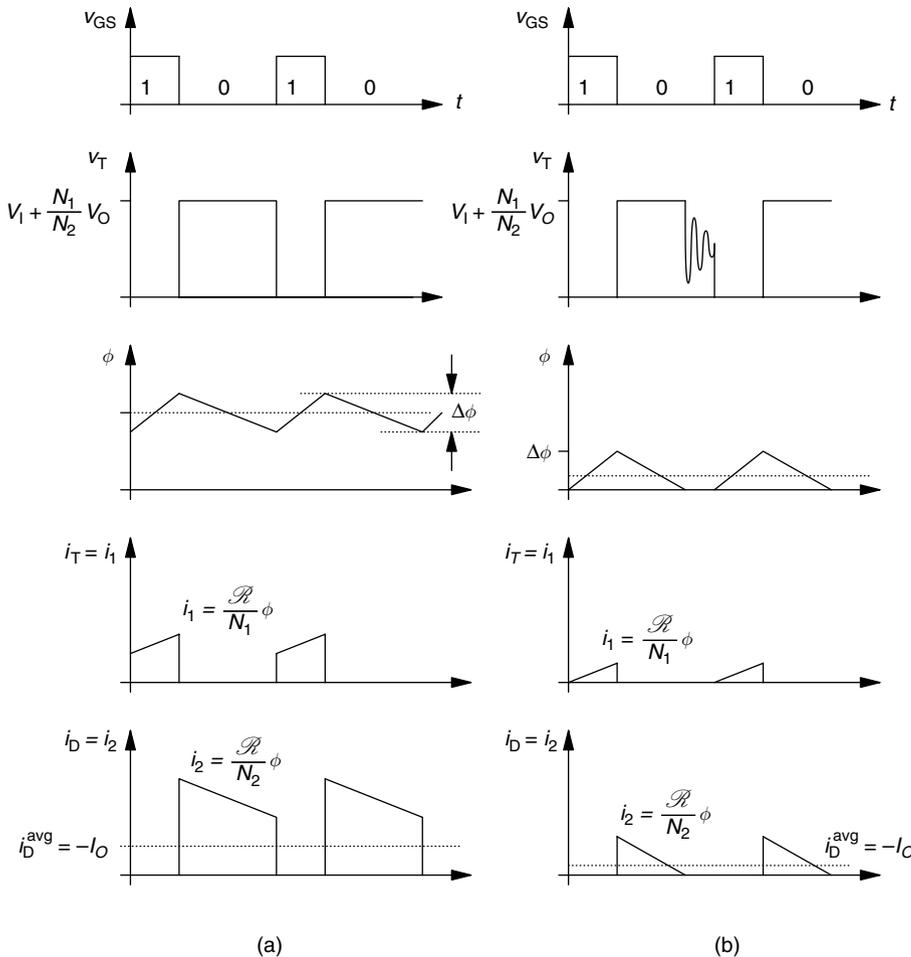
Figure 18.20   Flux, voltage and current waveforms of the isolated Flyback SMPS for (a) continuous and (b) discontinuous inductor flux
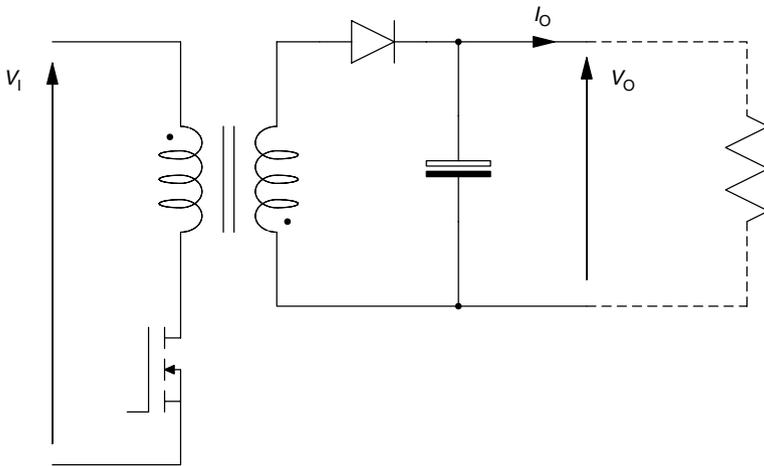
Figure 18.21 Normal arrangement of isolated Flyback SMPS
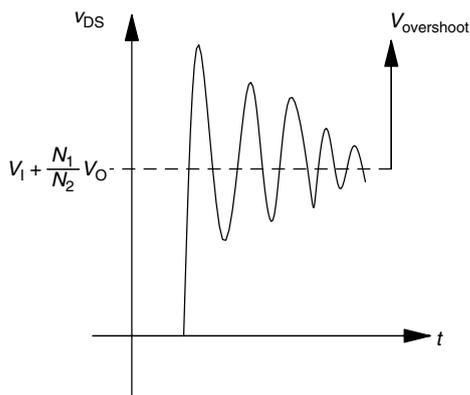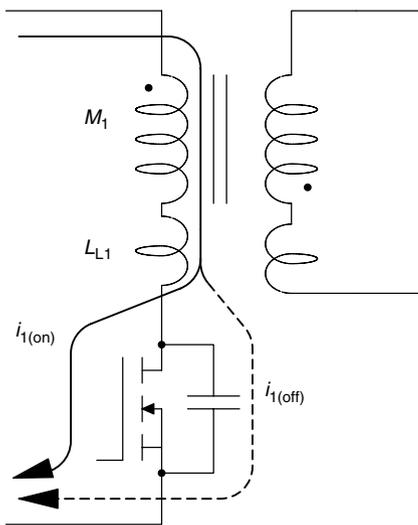
Figure 18.22 Overshoot of transistor voltage at turn-off

18.2.6 Transformer isolated buck SMPS

Some SMPS designs do not lend themselves to direct incorporation of a mutually coupled inductor. Instead, the energy storage function occurs in a single inductor and a further mutually coupled pair of inductors is introduced to provide isolation. This is illustrated by the isolated Buck SMPS circuits of *Figure 18.24*. All three versions of the circuit apply an isolated pulse train to the standard LC output stage of a Buck circuit. The transfer characteristic in each case is similar to the Buck SMPS with a scaling factor of the turns ratio of the transformer:

$$\frac{V_O}{V_I} = \frac{N_S}{N_P}\delta \tag{18.27}$$

The differences between the circuits are in the ratings of the transistors, the control of leakage energy and the utilisation of the magnetic core.

The circuit (*Figure 18.24(a)*) has a well-defined path in which to recover the primary leakage energy. It also causes the transformer flux to swing both positive and negative. Thus, the core can be utilised from its saturation limit in one direction to its saturation limit in the other. The transistors in the circuit can be rated for the input voltage with no significant overshoot. These three advantages are gained at the expense of using a 4-transistor full bridge. The duty-cycle should be defined as $(t_{on1} + t_{on2})/T$ for use in Equation 18.27 (where t_{on1} and t_{on2} are the times for which positive and negative voltage are applied to the primary; for the remaining time the voltage should be zero). It is essential to keep $t_{on1} = t_{on2}$ in order to avoid 'stair-case' saturation of the transformer core (small net increments of flux for each cycle of operation).

The circuit (*Figure 18.24(b)*) uses a bifilar primary winding to achieve bi-directional flux swings with only two transistors. However, the voltages reflected from one primary to the other require the transistors to support twice the input voltage during their off-state. Further, there is no path to discharge the primary leakage energy and voltage overshoot occurs. Again, the duty-cycle is defined by the sum of the two conduction periods for use in Equation 18.27.

The circuit (*Figure 18.24(c)*) (often known as the forward converter) uses only one transistor and can only create a unidirectional flux swing (thus requiring twice the core
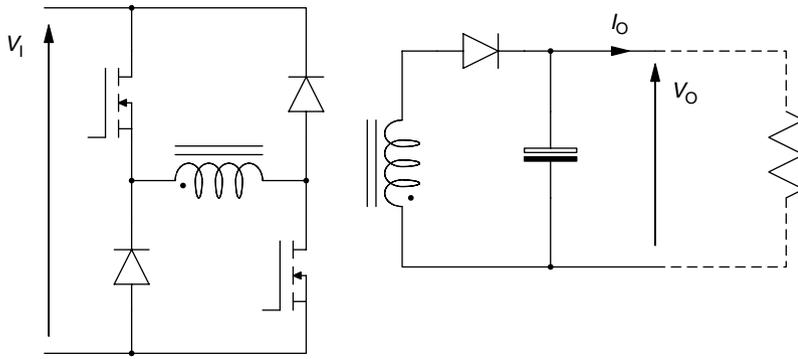
Figure 18.23 Half-bridge Flyback SMPS
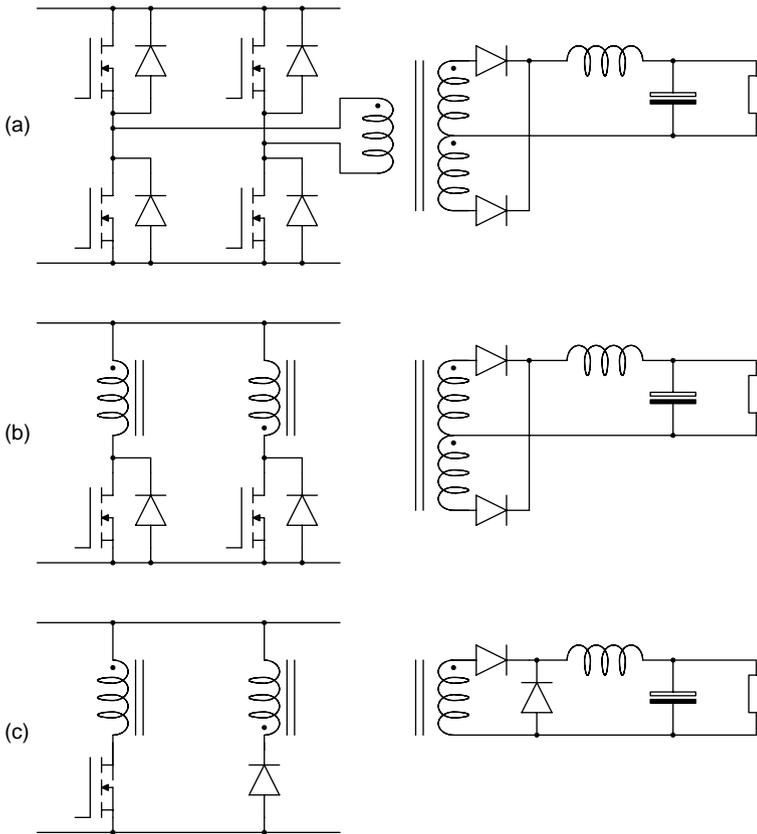
Figure 18.24 Isolated Buck SMPS: (a) full bridge; (b) push-pull and (c) forward

volume to hold off saturation for the same voltage and frequency conditions as the other circuits). The bifilar primary winding is there only to discharge the magnetising current of the transformer. There is no discharge path for the primary leakage energy and so voltage overshoot occurs.

18.2.7 SMPS control

It is rare to see a SMPS run in open loop. Closed loop operation is essential to ensure that the output voltage is accurately maintained at the desired value. The output voltage can be affected by changes in the output current or input voltage. There are several imperfections in practical SMPS that were not incorporated in the analysis of the previous sections such as voltage drops across the semiconductors and across the resistance of the inductor. The change from discontinuous to continuous mode will also affect the output voltage. All of these factors can be mitigated by feedback control. To achieve this we require a circuit that can vary, or modulate, the pulse-width applied to the transistor under the influence of some other signal. The usual approach is to use a triangle wave or saw-tooth
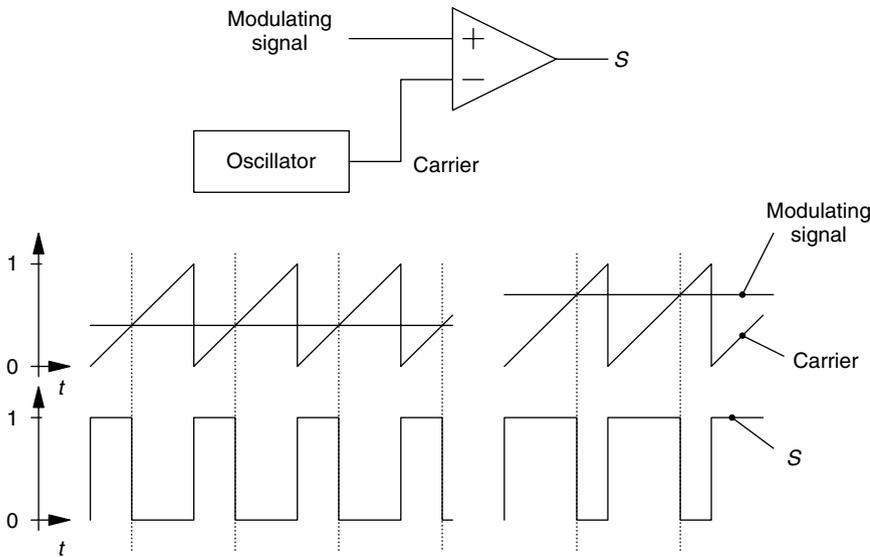
Figure 18.25 A pulse-width modulator with saw-tooth carrier

wave carrier. The carrier is compared with the modulating signal as shown in *Figure 18.25*. The comparator gives a high output whenever the modulating signal is greater than the carrier and thus produces pulses with a width proportional to the modulating signal.

A schematic of the closed loop system is shown in *Figure 18.26*. The forward transfer function, $F(s)$ of the system is complex. The modulator is linear over its normal range but saturates outside that range. The SMPS circuit is time varying because it has two operating modes. Even in continuous mode, most SMPS have a non-linear transfer function. The parasitic components of the circuit, particularly the ESR of the output capacitor, can form significant terms in the transfer function of the circuit. The output voltage is normally found to decrease as output current is drawn (because of the increased voltage drop across resistances and semiconductors in the circuit). Variation of the input voltage forms a further disturbance input to the system.

On a simple view, the application of feedback solves many of these problems. The closed loop transfer function, taking into account the two disturbance terms, is:

$$v_O(s) = \frac{C(s)F(s)}{1 + C(s)F(s)G(s)} \cdot v_R(s)$$
$$+ \frac{D_1(s)}{1 + C(s)F(s)G(s)} \cdot v_I(s) \qquad (18.28)$$
$$+ \frac{D_2(s)}{1 + C(s)F(s)G(s)} \cdot i_O(s)$$

Provided that the loop gain of the system, $C(s)F(s)G(s)$, is large, then the disturbances are largely rejected. Further, the transfer function (from reference to output) is dominated by the feedback attenuator, $G(s)$. The feedback attenuator is normally a potential divider and has a simple linear gain.

$$v_o(s) \approx \frac{1}{G(s)} \cdot v_R(s)$$
$$\approx k v_R(s) \qquad (18.29)$$

where k is the reciprocal of the feedback gain.
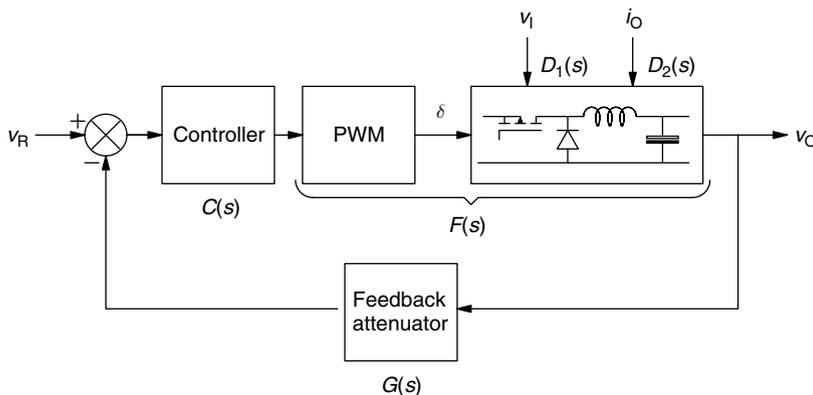
Figure 18.26 A closed loop controller schematic for an SMPS
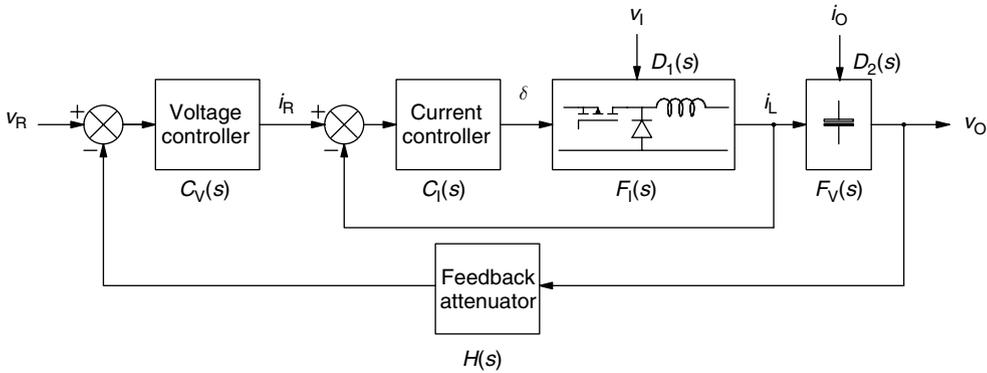
Figure 18.27 Current mode control using nested control loops

The control element $C(s)$ must be chosen with care to ensure stability. Techniques such as state-space averaging[3] can be used to derive linearised dynamic models of the SMPS circuits to facilitate such design. (Note that the transfer characteristics, as functions of δ, derived elsewhere in Section 18.2 express only the steady-state properties of the circuits.)

The usual elements of a controller for an SMPS (that is, a pulse-width modulator, error amplifier, an adjustable gain and a gate drive circuit) are available as standard integrated circuits. Often included is some form of current limit. A low value resistor placed in the ground line of the supply is used to monitor the current. Above some threshold value, the pulse-width of the gate-drive is reduced to reduce the output voltage and limit the current.

The non-linear, time-varying nature of the SMPS makes controller design problematic and it is often difficult to ensure stability across a wide range of operating conditions. A technique that can alleviate the problems is known as current-mode control. It is based on the feedback of two signals, in this case through two nested control loops, *Figure 18.27*.

The choice of nested loops follows from recognising that the rate of change of inductor current is much higher than the rate of change of output voltage. Therefore, the inductor current can be controlled in a fast inner loop and the output voltage is controlled in a slower outer loop. If the inner loop tracks the current reference accurately then the outer loop becomes first-order dominated and is relatively easy to design.

The generation of pulses to drive the transistor is somewhat different from the voltage control case. The current demand set by the outer loop forms a reference. The transistor is turned on at regular intervals and stays on until the current ramps up to the reference level. The transistor then remains off until the next of the regular turn-on events. Thus, the inductor current is controlled within each switching cycle.

A further advantage of current mode control is that feed-forward of input voltage disturbances can be applied readily. There is a stability issue to be addressed at duty-cycles of greater than 1/2, however, this can be overcome by a method known as slope-compensation.[3]

18.3 D.c./a.c. conversion

18.3.1 Single phase bridge

The full-bridge circuit was introduced in Section 18.2.1.1 as a way of converting d.c. to $\pm$d.c. It was used again in Section 18.2.6 to create a bi-directional voltage on the primary of a transformer. We can use the same circuit (repeated but re-labelled here as *Figure 18.28*) to convert d.c. to a.c. We can control the duty-cycle of the switches to produce a waveform with an average that gradually increases in a positive
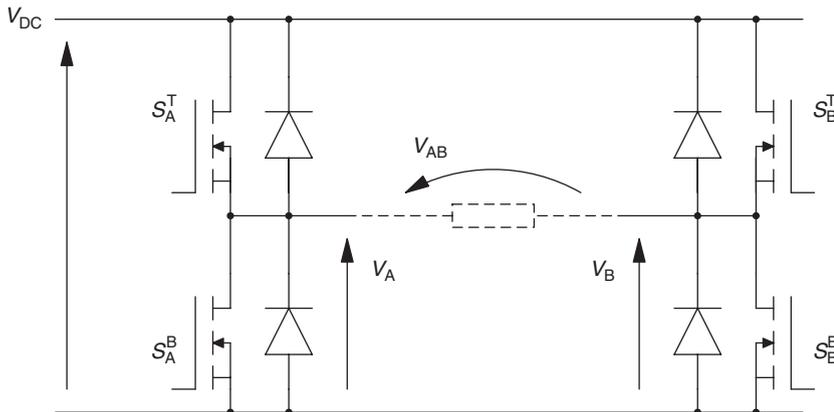
Figure 18.28 Full bridge with switching signal assignment of *Figure 18.30*
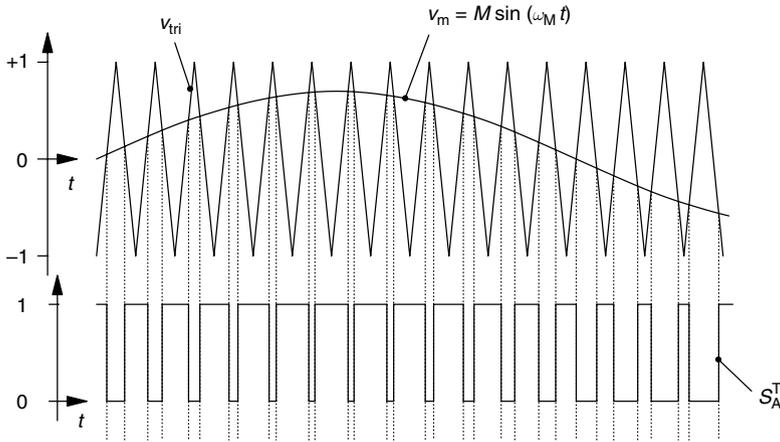
Figure 18.29 Sinusoidally modulated pulse-widths

sense and then decreases and turns negative, *Figure 18.29*. The duty-cycle is modulated as:

$$\delta = \tfrac{1}{2} + \tfrac{1}{2}M \sin(\omega_M t) \quad \text{where } 0 \leq M \leq 1 \tag{18.30}$$

where M is known as the depth of modulation and will set the magnitude of the a.c. voltage being synthesised.

Top and bottom switches, such as S_A^T and S_A^B, will be operated in anti-phase but not strictly so. Because each switch takes time to turn off and time to turn on, it is important to initiate turn-off of one switch before turn-on of the other. This avoids both switches being partially on at the same time and providing a shoot-through path between the supply rails. This is known as providing dead-time or under-lap.

As indicated in *Figure 18.29*, the modulation of the duty-cycle can be performed through a comparison of the desired sinewave with a triangular carrier. An analogue circuit similar to that described in Section 18.2.7 could be used. It is more common for an inverter (d.c./a.c. converter) to be controlled with a microcontroller or digital signal processor, DSP. The transistors are switched using the timer channels of the processor. The sinewave modulation is achieved by regularly updating the timer values with times calculated using a look-up table of sinewave samples. Scaling the sine-wave data controls the magnitude of the output voltage. The rate at which progress is made through the sinewave look-up table determines the frequency of the sinewave synthesised at the output.

It is common to phase shift the carrier waveform of the two sides of the bridge as shown in *Figure 18.30*.

The output voltage waveforms are also shown in *Figure 18.30*. Each side of the bridge can be switched between $+V_{DC}$ and 0. The voltage appearing across the output can be $+V_{DC}$, 0 or $-V_{DC}$. These waveforms are known as two-level and three-level pwm respectively. It can be seen that in the case of a phase-shifted carrier the 3-level waveform has twice the frequency of the carrier.

The low-frequency components of these voltages are:

$$v_{A0} = \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M \sin(\omega_M t)$$
$$v_{B0} = \tfrac{1}{2}V_{DC} - \tfrac{1}{2}V_{DC}M \sin(\omega_M t) \tag{18.31}$$
$$v_{AB} = V_{DC}M \sin(\omega_M t)$$
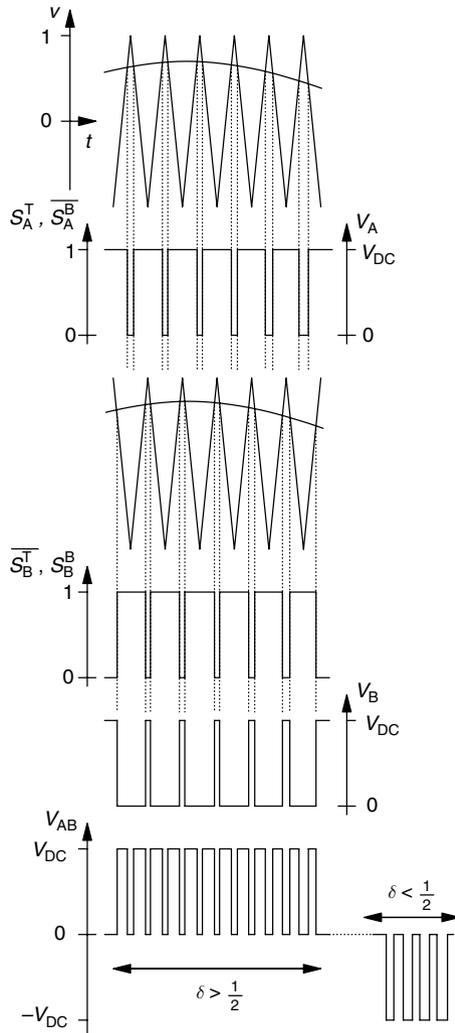
Figure 18.30 Phase-shifted carrier used to interleave PWM of left- and right-hand sides of full bridge.
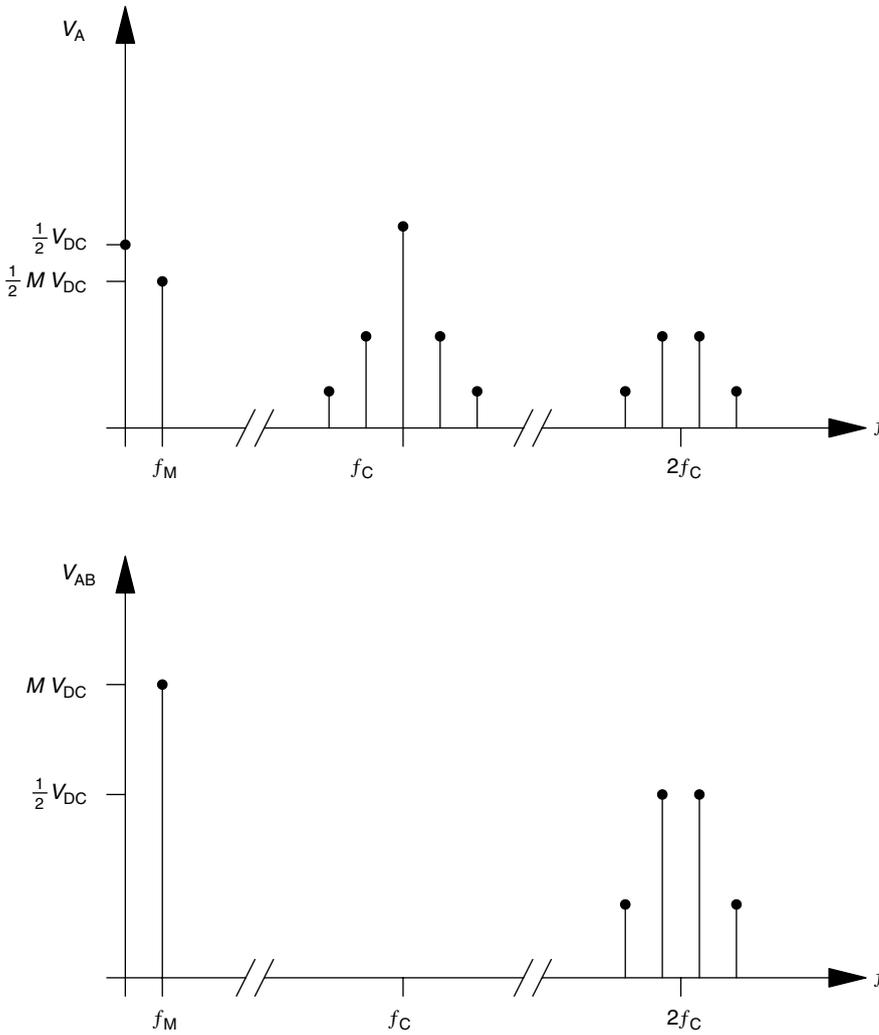
Figure 18.31   Frequency spectra of a half bridge voltage and a full bridge voltage with phase-shifted carrier

The d.c. portions of the voltage at each half of the bridge are common mode and do not appear in the output voltage.

The objective of this circuit is to produce sinusoidal voltage but what we have is a sinusoidally modulated rectangular wave. The difference is illustrated in the frequency spectra of *Figure 18.31*. The details of the spectra depend on how the modulation was implemented, but the basic form shown here is typical.

18.3.2   Three phase bridge

For most three-phase applications, the requirement is to produce a balanced set of voltages for a three-wire system. In this case, a pair of transistors is used to produce an a.c. waveform for each phase voltage. The common mode (or zero-sequence) d.c. component is unimportant in a three-wire system.

The three phase voltages V_A, V_B and V_C are modulated to give a balanced three-phase set:

$$
\left.
\begin{aligned}
v_A &= \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin(\omega t) \\
v_B &= \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin\left(\omega t - \tfrac{2\pi}{3}\right) \\
v_C &= \tfrac{1}{2}V_{DC} + \tfrac{1}{2}V_{DC}M\sin\left(\omega t + \tfrac{2\pi}{3}\right)
\end{aligned}
\right\}
\tag{18.32}
$$

$$
\left.
\begin{aligned}
v_{AB} &= \tfrac{\sqrt{3}}{2}V_{DC}M\sin\left(\omega t + \tfrac{\pi}{6}\right) \\
v_{BC} &= \tfrac{\sqrt{3}}{2}V_{DC}M\sin\left(\omega t - \tfrac{\pi}{2}\right) \\
v_{CA} &= \tfrac{\sqrt{3}}{2}V_{DC}M\sin\left(\omega t + \tfrac{5\pi}{6}\right)
\end{aligned}
\right\}
\tag{18.33}
$$

All three phases are modulated using the same carrier and so there is no doubling of the effective switching rate as in
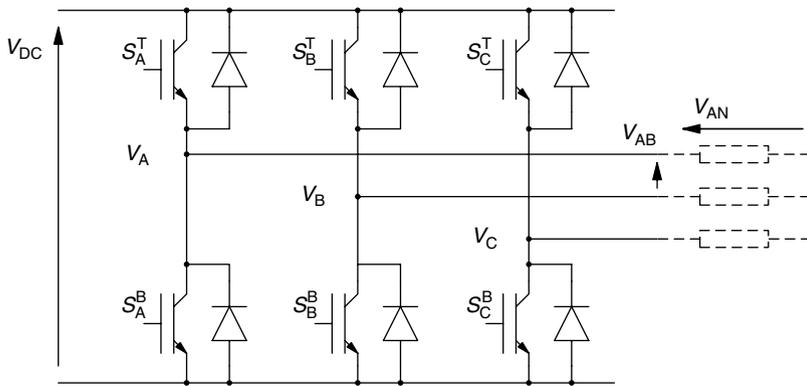
Figure 18.32 A three-phase inverter bridge
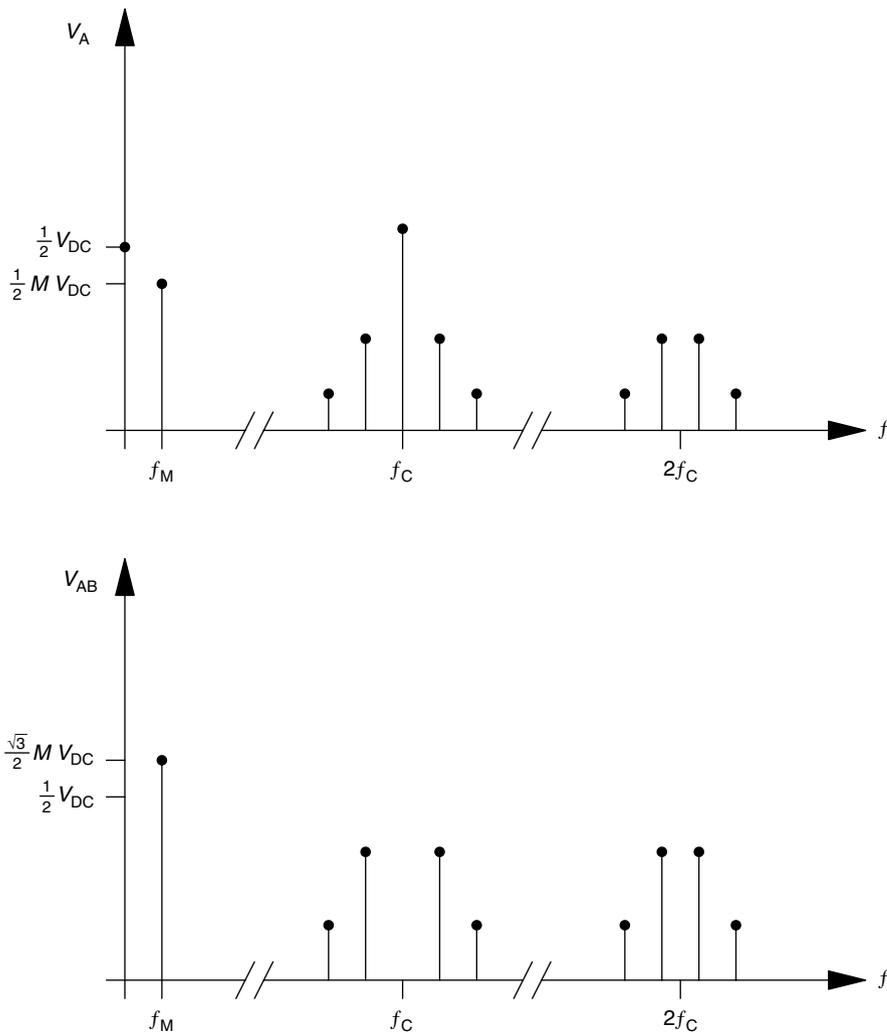
Figure 18.33 Frequency spectra of the phase and line voltages of the three-phase inverter of *Figure 18.32*
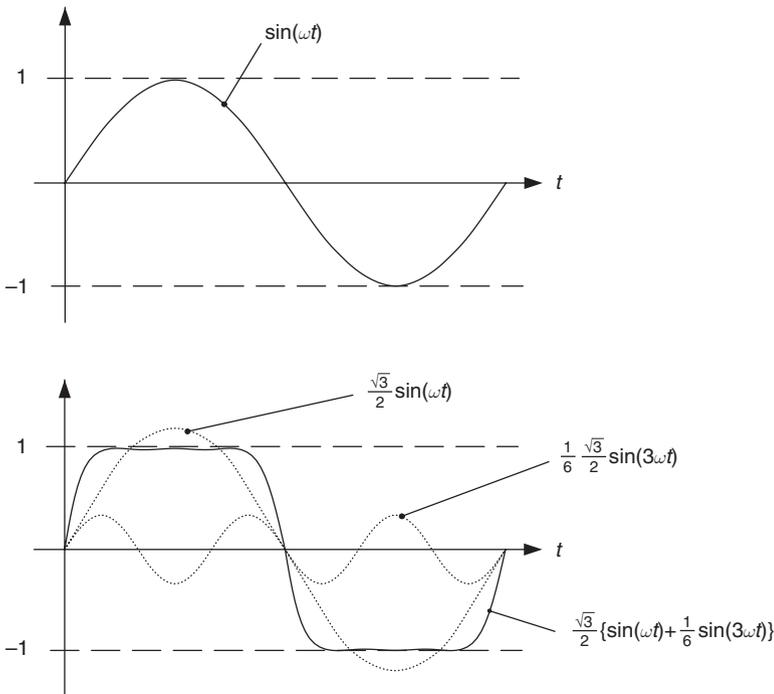
Figure 18.34   Increase of maximum fundamental by addition of third harmonic

the single-phase bridge. However, the carrier component is zero-sequence and will not appear in the line voltages to the phase voltages at the load. The frequency spectra of the phase and line voltages are shown in *Figure 18.33*.

The fact that zero-sequence components can be inserted into the inverter phase voltage waveforms without affecting the line voltage waveforms can be useful. The peak line voltage indicated above is $\sqrt{3}/2V_{DC}$. It should be possible to achieve a peak line voltage of V_{DC} by switching on the top switch of one phase and the bottom switch of another. This can be realised for a sinewave pattern by including a zero-sequence third harmonic set in the waveforms as shown in *Figure 18.34*. The fundamental component can be boosted by $2/\sqrt{3}$ without exceeding a duty cycle of unity if the third harmonic is 1/6th of amplitude of the fundamental.

There is an alternative way of forming the switching waveforms of the inverter known as space-voltage vector modulation, SVM. It is based on the fact that there are only eight useful states of the inverter as indicated in *Table 18.1*. When a bottom switch is on, the voltage of that phase will be zero; and when a top switch is on, the voltage of that phase will be V_{DC}. We discount states where neither or both of the switches in a phase are on. The zero sequence voltage is the average of the three phase voltages. The overall voltage output of the inverter is represented as a space-voltage vector. That is, the voltage of each phase is taken to have a spatial position matching the spatial positioning of the phase windings in an electrical machine. This is equivalent to a Clarke transform[4] to $\alpha\beta\gamma\varsigma$co-ordinates:

Table 18.1   Inverter states and resultant space-voltage vector

State	Switches on			Phase voltages			Zero sequence $V_{\gamma\varsigma}=V_N$	Space-voltage vector V
	A	*B*	*C*	V_A	V_B	V_C		
0	*B*	*B*	*B*	0	0	0	0	0
1	*T*	*B*	*B*	V_{DC}	0	0	$\frac{1}{3}V_{DC}$	$V_{DC}\angle 0°\Leftarrow$
2	*T*	*T*	*B*	V_{DC}	V_{DC}	0	$\frac{2}{3}V_{DC}$	$V_{DC}\angle 60°\Leftarrow$
3	*B*	*T*	*B*	0	V_{DC}	0	$\frac{1}{3}V_{DC}$	$V_{DC}\angle 120°\Leftarrow$
4	*B*	*T*	*T*	0	V_{DC}	V_{DC}	$\frac{2}{3}V_{DC}$	$V_{DC}\angle 180°\Leftarrow$
5	*B*	*B*	*T*	0	0	V_{DC}	$\frac{1}{3}V_{DC}$	$V_{DC}\angle 240°\Leftarrow$
6	*T*	*B*	*T*	V_{DC}	0	V_{DC}	$\frac{2}{3}V_{DC}$	$V_{DC}\angle 300°\Leftarrow$
7	*T*	*T*	*T*	V_{DC}	V_{DC}	V_{DC}	V_{DC}	0
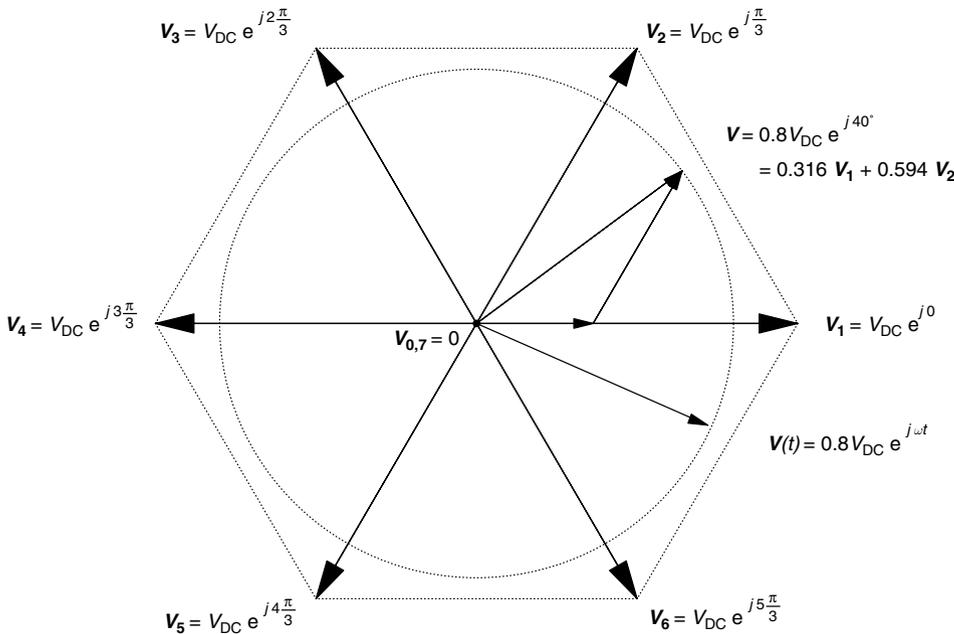
Figure 18.35 Space-voltage vectors of a three-phase inverter and synthesis of a voltage trajectory by space-voltage vector modulation

$$V = V_{AN} + V_{BN}e^{j\frac{2\pi}{3}} + V_{CN}e^{-j\frac{2\pi}{3}}$$

or

$$V = V_{\alpha\varsigma} + jV_{\beta\varsigma} \qquad (18.34)$$

$$\begin{bmatrix} V_{\alpha\varsigma} \\ V_{\beta\varsigma} \\ V_{\gamma\varsigma} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}$$

The normal objective is to produce a smoothly rotating space-voltage vector and, by implication, produce line voltages that are a balanced three-phase set. *Figure 18.35* shows the desired trajectory of the space-voltage vector. To achieve the point on the trajectory shown (a circle of radius 0.8 V_{DC} in this example) we combine the nearest two non-zero space-voltage vectors with the two zero space-voltage vectors.

For example, to achieve $V = 0.8\ V_{DC} \angle 40°$ we use states 0, 1, 2, 7.

The duty-cycles of the two non-zero space-vectors must satisfy:

$$\delta_2 V_{DC}\sin(60°) = 0.8V_{DC}\sin(40°)$$
$$\delta_1 V_{DC} + \delta_2 V_{DC}\cos(60°) = 0.8V_{DC}\cos(40°)$$

Thus, in this case, $\delta_2 = 0.594$ and $\delta_1 = 0.316$. The remaining time within the period, $\delta_0 = (1 - \delta_1 - \delta_2)$ is split equally between the two zero-voltage states; states 0 and 7. A useful switching sequence, because it minimises the number of switch transitions and returns to the original state, is:

State 0 for T$\delta_0/4$
State 1 for T$\delta_1/2$
State 2 for T$\delta_2/2$

State 7 for T$\delta_0/2$
State 2 for T$\delta_2/2$
State 1 for T$\delta_1/2$
State 0 for T$\delta_0/4$

The sum of the duty-cycles of the two non-zero states is constrained to less than or equal to unity. This means that the synthesised space-voltage vector must lie within the hexagonal limit shown in *Figure 18.35*. The maximum radius circle that can be accommodated is $\frac{\sqrt{3}}{2}V_{DC}$ which is equivalent to the maximum amplitude sinewave that can be synthesised with simple PWM employing third-harmonic injection.

In high-power applications, particularly large machine drives, the switching frequency may be very low compared to the required sinewave to be synthesised. Special techniques are required involving synchronising the carrier to the sinewave or optimising individual switching times to reduce harmonic distortion. For very large inverters the devices might only be switched at line frequency in what is known as six-step or quasi-square operation. This is illustrated in Section 19.3.4.1 'Six-step square-wave inverter'.

18.3.3 Current source inverters

There are occasions on which a three-phase current set is required rather than a three-phase voltage set. A class of circuits, known as current source inverters,[6] exist which are duals of the circuits discussed in Section 18.3.2. The d.c.-side is supplied with a current via a smoothing inductor. The output can be pulse-width modulated or simply switched as a low frequency rectangular wave. Such circuits are sometimes used in large thyristor based drive systems as discussed in Section 19.3.4.2 'Current source inverters'. There are difficulties in designing a d.c.-side inductor with low resistance and high saturation limit. To achieve a

fast-response controlled current it is normally better to use a voltage source inverter with a local current control-loop.

18.4 A.c./d.c. conversion

A.c./d.c. conversion is commonly referred to as rectification. There are well-established rectifier circuits based on diodes but these circuits suffer limitations. They have poor output voltage regulation characteristics and offer no adjustment of output voltage. They also generate harmonically distorted current in the a.c. system. Standards, such as IEC 1000 (adopted as EN 61000 in the EU), place limits on such distortion and lead to the adoption of more sophisticated circuits. The tightest limits imposed by these standards are on even-order harmonic current. This all but prohibits the use of half-wave circuits that draw current during only one half-cycle of the a.c. waveform.

18.4.1 Line-frequency-switched rectifiers

The single-phase full-wave diode bridge rectifier is shown in *Figure 18.36*. The diodes can be considered in pairs: one pair (D_A^T and D_B^B) applies the positive half-cycle of the a.c. to the load and the other (D_B^T and D_A^B) applies the negative half-cycle. The three-phase bridge rectifier of *Figure 18.37* is an extension of the single-phase bridge with three pairs of diodes. The line voltage that is highest in magnitude (whether positive or negative) is applied to the load. Each

diode conducts for a third of a cycle and shares that conduction period with opposite side diodes from the two other phases.

The general form of load on the d.c.-side of a bridge rectifier is inductive-resistive impedance and a d.c. voltage. This is a reasonable representation of both the armature of a d.c. machine or large valued 'reservoir' capacitor (with either significant ESR and ESL or added inductance). *Figure 18.38* shows a single-phase example. The diodes of this circuit will begin to conduct at angle α when the magnitude of the a.c. voltage exceeds the voltage on the d.c.-side. Once in conduction the current is dictated by a first order differential equation.

$$L\frac{\mathrm{d}i}{\mathrm{d}t} = |v_I| - iR - E \qquad (18.35)$$

The current rises while the a.c. voltage exceeds the sum of E and iR and falls thereafter. When the current reaches zero, the diodes fall out of conduction. The current will re-establish at $\pi + \alpha$ in the next half cycle. The extinction angle, β can be found from the 'equal area' criterion as shown in *Figure 18.38*. In other words, β can be found by solving:

$$\int_{\alpha}^{\beta} \frac{\hat{V}_I \sin(\omega t) - iR - E}{L} \cdot \mathrm{d}t = 0 \qquad (18.36)$$
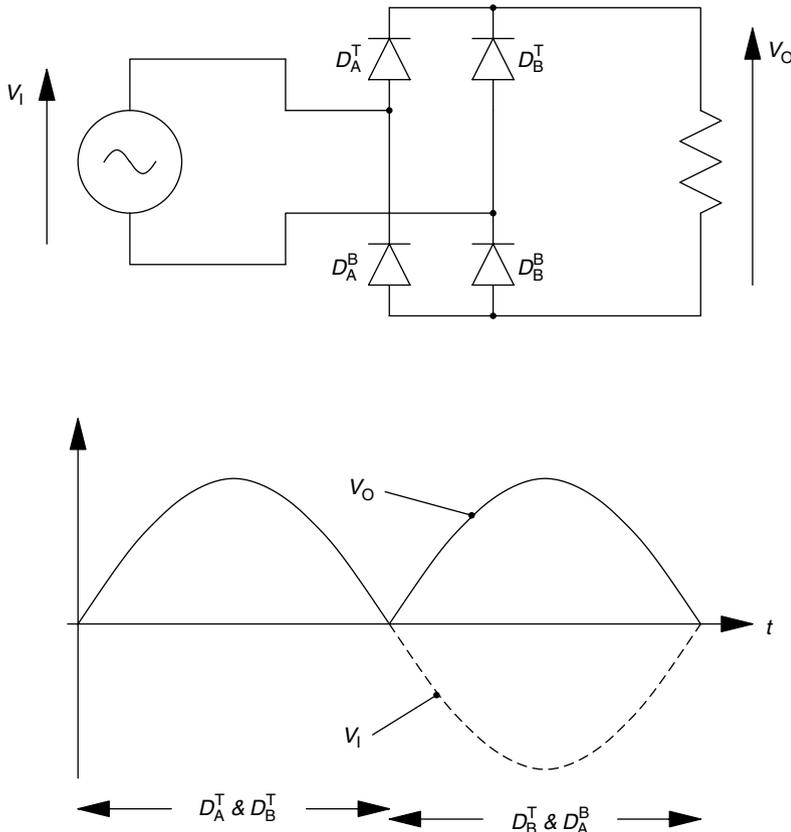
Figure 18.36 Single-phase rectifier with resistive load
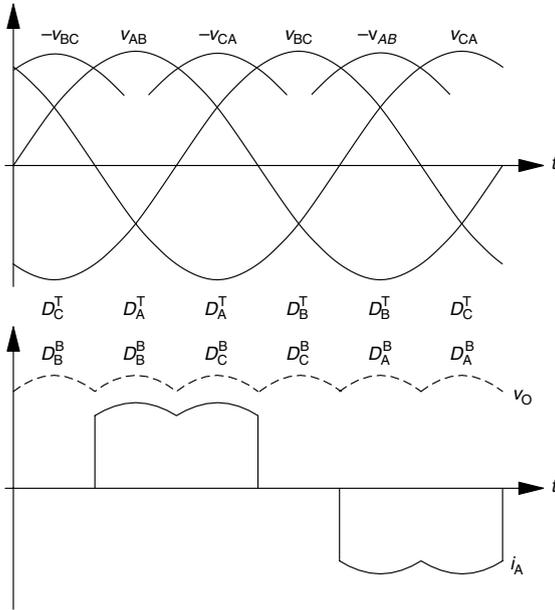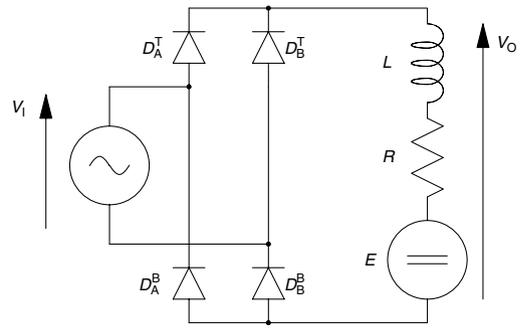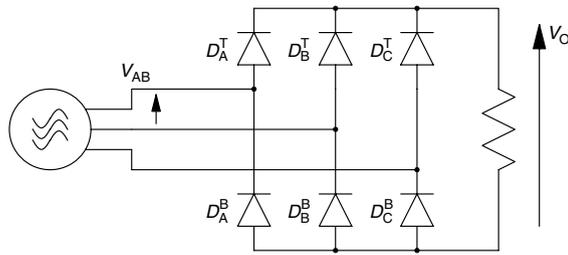
Figure 18.37 Three-phase rectifier with resistive load

The solution must be found numerically. Using β we can also find the average voltage applied to the load:

$$V_{\mathrm{O(avg)}} = \frac{\hat{V}_{\mathrm{I}}}{\pi} \left(\cos(\alpha) - \cos(\beta) \right) + E \left(1 - \frac{\beta - \alpha}{\pi} \right) \right] \quad (18.37)$$

If the current becomes continuous then the first pair of diodes conducts from α to $\pi + \alpha$. The output voltage is found by replacing β with $\pi + \alpha$.

$$V_{\mathrm{O(avg)}} = \frac{2\,\hat{V}_{\mathrm{I}}}{\pi} \cos(\alpha) \quad (18.38)$$

A variant of this circuit is obtained by substituting thyristors for the diodes, *Figure 18.39*. It is now possible to delay the onset of conduction, α_1 beyond the point α at which conduction is first possible.

$$\alpha = \sin^{-1} \left(\frac{E}{\hat{V}_{\mathrm{I}}} \right) \right] \quad (18.39)$$
$$\alpha \le \alpha_1 < \pi - \alpha$$

The analysis of the diode circuit can be applied again and it is seen that the average voltage appearing across the load can now be varied.
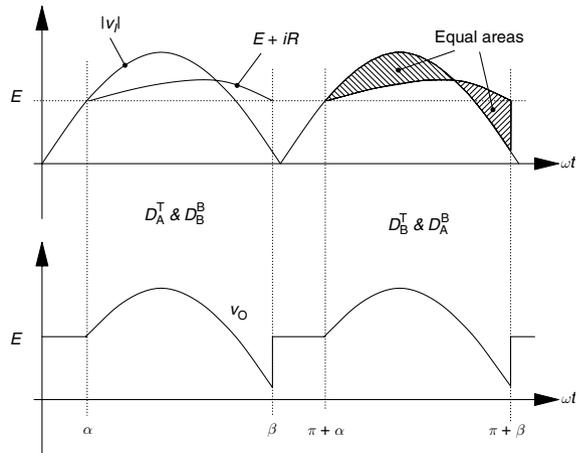
Figure 18.38 Single-phase rectifier with ERL load

For some loads, notably d.c. machines, it is possible to make E negative and it then becomes possible to transfer power from the d.c.-side to the a.c.-side. This can provide regenerative braking of a machine as discussed in Section 19.2.1 'D.c. Motor Drive Systems'. Initiation of conduction is delayed such that current flow is predominantly in the following half-cycle. The power on the d.c.-side is negative since the current is positive while the voltage E is negative. The power on the a.c.-side is also negative (on average) since, for instance, positive current flows during the negative half-cycle. The negative power indicates a reversal of flow from the assumed direction.

The three-phase versions of the bridge exist such as *Figure 18.40*. Many variations of the rectifier bridge exist based on full or partial replacement of diodes with thyristors. Such circuits are well known for use in high power drives as discussed in Section 19.3.1 'A.c. to d.c. Power Conversion'.

The circuit of *Figure 18.40* has an average output voltage (in continuous conduction) of:

$$V_{\mathrm{O(avg)}} = \frac{3\hat{V}_{\mathrm{I}}}{\pi} \cos(\alpha) \quad (18.40)$$

where $\hat{V}_{\mathrm{I}}$ is the peak line voltage and α is measured from the cross-over of two line voltages.

These circuits have been popular choices for the supply of d.c. machines from a.c. sources because of the control possibilities they offer. Their use is waning because d.c. machines
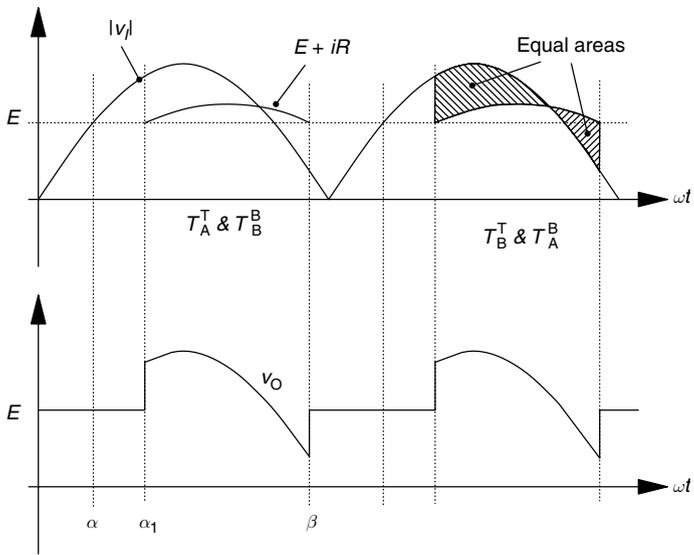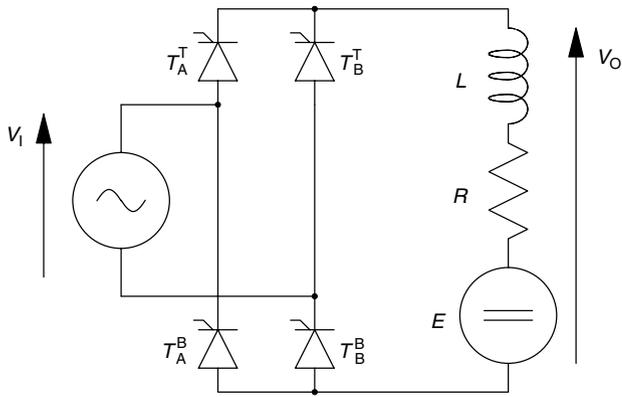
Figure 18.39 Single-phase thyristor rectifier
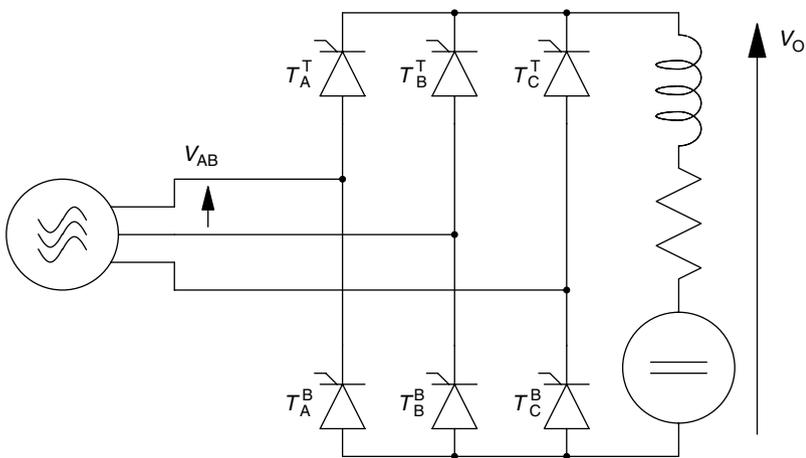
Figure 18.40 Three-phase fully-controlled thyristor rectifier

are losing ground to a.c. machines. Even where d.c. machines are used, other power conversion circuits may be sought because the non-sinusoidal a.c.-side current of these line-frequency-switched rectifiers are problematic. Phase-angle controlled thyristor rectifiers will continue to be used at very high powers where thyristors are the only viable devices and the costs of harmonic mitigation can be met.

18.4.1.1 Non-sinusoidal a.c.-side current

Figure 18.41 shows the results of a circuit simulation of a rectifier like that of *Figure 18.40* operated such that the thyristors turn-on 18° after the cross-over of the line voltages. The line voltages were 415 V at 50 Hz. The frequency spectrum shows that there are no even harmonics (as expected of a full wave rectifier with symmetric current wave-shape in the two half cycles). There are also no triplen harmonics (i.e. harmonics of order $3k$ with k any integer) as there is no path for these zero-sequence harmonics. The harmonics present are of order $6k \pm 1$ and this is characteristic of a six-pulse rectifier.

Table 18.2 compares the harmonic amplitudes found in this example circuit with the amplitudes allowed by the standard IEC 1000-3-3.

The fundamental amplitude is recorded as 15.3 A (peak) and so falls within the scope of class-A of IEC 1000-3-3, which applies up to 16 A (RMS). As expected, the largest amplitude emissions are the 5th, 7th and 11th harmonics and, in fact, the converter exceeds the Class-A limits at these points. Harmonic mitigation in the form of filtering or multi-pulse operation (Section 18.7.2 and Paice) may be sufficient to meet IEC 1000. If not, then a rectifier with active waveshape control (Section 18.4.2) will be needed.

Supply waveforms such as those in *Figure 18.41* need to be treated carefully when discussed in terms of the power factor. The original definition of power factor, as the ratio of real power to apparent power, must be used and any derived terms, based on sinusoidal conditions, must be ignored. A useful set of definitions follows if the a.c. voltage can be assumed to be perfectly sinusoidal even if the current is not. It then follows that only the in-phase fundamental frequency component of the current transfers real power. All harmonic currents cause oscillating instantaneous power flow that average to zero.

$$P = V_{RMS} I_{1,RMS} \cos(\theta) \Leftarrow \tag{18.41}$$

where $I_{1,RMS}$ is the RMS value of the fundamental frequency component of current and θ is the displacement angle between that component of current and the voltage.

This leads to the following definition of power factor:

Power factor = Distortion factor × Displacement factor

$$\tag{18.42} \Leftarrow$$

where   Distortion factor $\mu = \dfrac{I_{1,RMS}}{I_{RMS}} \Leftarrow$

and   Displacement factor = $\cos(\theta) \Leftarrow$

$$P = V_{RMS} \, I_{RMS} \mu \cos(\theta) \tag{18.43} \Leftarrow$$

18.4.2 Wave-shape controlled rectifiers

Just as switch-mode techniques are used to create sinewave supplies from d.c. sources, so they can be used to transform sinewave input currents into d.c. current. Various topologies of power converter exist but the one that has gained greatest acceptance in practice is derived from the Boost SMPS. *Figure 18.42* shows the d.c./d.c., 1-phase/d.c. and 3-phase/d.c. variants of the Boost converter. In each circuit, a switch (or switches) can be turned on to provide current path-A that imposes a positive voltage across the inductor and increases the current. Power is taken from the input and is stored in the inductor. The switch can be turned off and current path-B is established. A negative voltage is imposed across the inductor and the current reduces. Energy is transferred from both the input and the inductor to the capacitor, and the capacitor voltage rises.

Two control tasks exist; one to regulate the output voltage and the other to control the increase and decrease of current in order to form a sinewave. Circuits operated in this fashion are often referred to as power factor correctors. They produce a distortion factor (and displacement factor) close to unity in a rectifier that would otherwise have a low power factor.

Table 18.2 Comparison of simulated circuit with harmonic limits

Harmonic order	Frequency (Hz)	Current amplitude (A)	IEC 1000 class-A (A)	Pass/fail
1	50	15.330	—	—
2	100	0.013	1.080	Pass
3	150	0.014	2.300	Pass
4	200	0.009	0.043	Pass
5	250	9.472	1.140	Fail
6	300	0.011	0.300	Pass
7	350	5.350	0.770	Fail
8	400	0.010	0.230	Pass
9	450	0.017	0.400	Pass
10	500	0.010	0.180	Pass
11	550	0.454	0.300	Fail
...				
38	1900	0.008	0.048	Pass
39	1950	0.016	0.058	Pass
40	2000	0.007	0.046	Pass
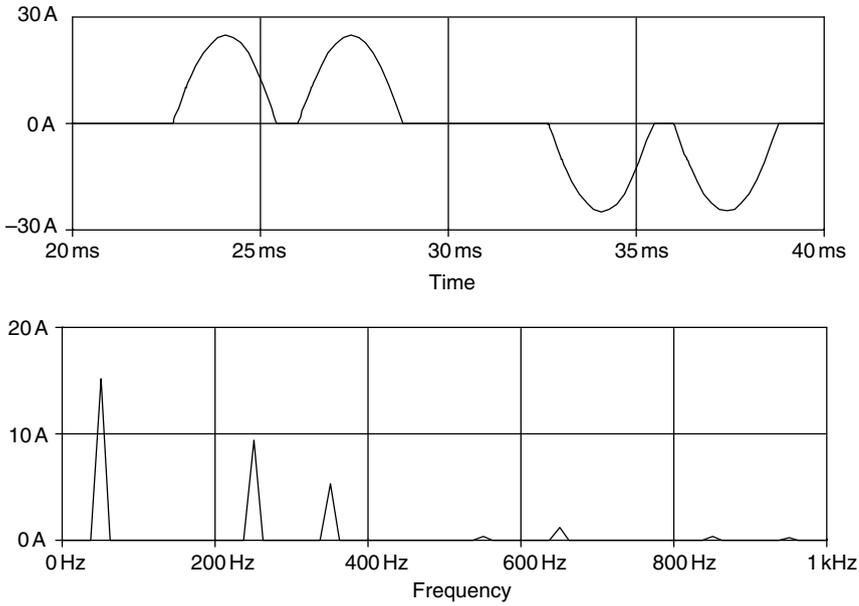
Figure 18.41   A.c.-side current of a thyristor bridge in time and frequency domain
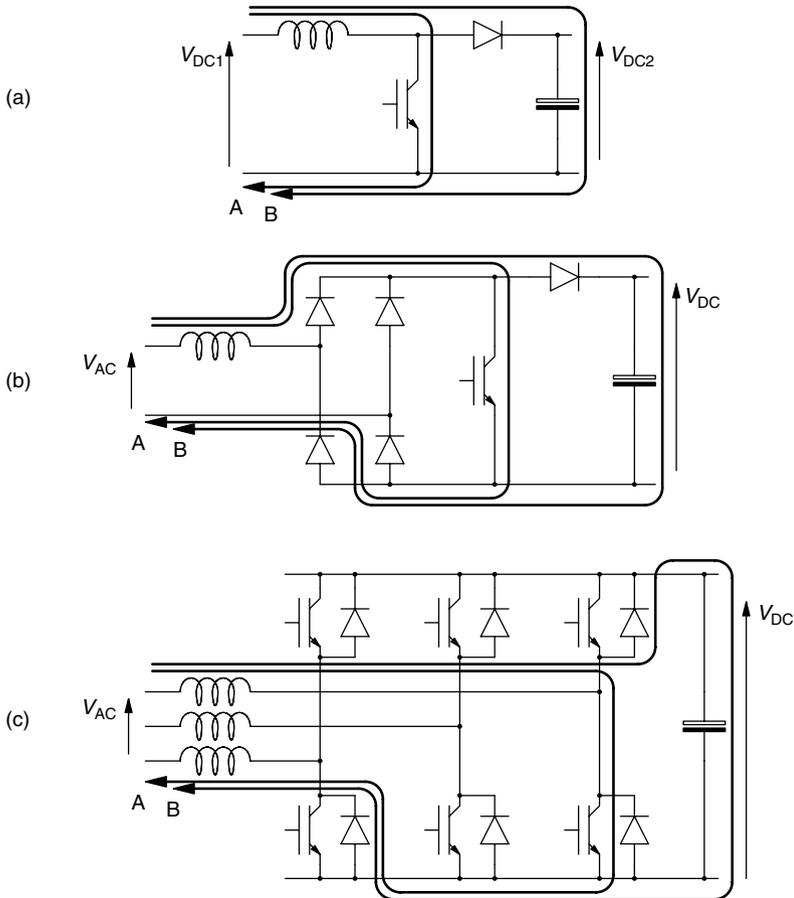
Figure 18.42   Boost SMPS in d.c./d.c., 1-phase/d.c. and 3-phase/d.c. forms

18.4.2.1 Single-phase

The Boost topology is advantageous because it places an inductor in series with input. Thus, the input current can be continuous and composed of a sinusoid with a small ripple superimposed. The step-up of voltage is not normally desired so a second stage step-down converter (such as a Buck or Flyback) is often added. Clearly, this adds expense and the double processing of power means it is also less efficient than a single stage converter[1]. However, the Boost circuit plus second-stage is considered the best solution where good a.c.-side waveform quality is required. The circuit of *Figure 18.43* is similar to that of *Figure 18.42(b)* except that the inductor has been relocated to allow all the required control signals to be referenced to the same potential.

Control of the converter is split into two sections. The first measures the output voltage error and sets a current demand that will correct it. The second stage takes the current demand, creates from it a sinusoidal current reference and modulates the switch to obtain such a current. The circuit is similar to a standard Boost SMPS but with a full-wave rectified input voltage. The duty-cycle is modulated to keep the output voltage constant while the input voltage varies. The sinusoidal reference shape is obtained by measuring the (full-wave rectified) instantaneous voltage.

It is inevitable that there is some distortion of the current immediately following the zero-crossing of the voltage because the input voltage is insufficient to increase the inductor current quickly enough to follow the sinusoidal reference. Careful design can reduce this distortion to the point where the harmonic content is small and standards such as IEC 1000 can be met with ease.

This has become a popular topology and several manufactures produce ICs that include these control functions. Two variants exist, as illustrated in *Figure 18.44*. The first uses a hysteresis controller for the current loop and results in fast response but a varying switching frequency. The second uses fixed-frequency PWM. The spread spectrum resulting from a varying switching frequency can make filter design difficult but it does have the advantage of spreading emissions thinly over a range rather than producing high level emissions concentrated at particular frequencies.

The control loop for the output voltage must be designed with a limited bandwidth typically around 5 Hz. The energy drawn from a single-phase supply will vary at twice line frequency even if sinusoidal current wave-shape is achieved. Thus, there will be an unavoidable output voltage ripple at twice line frequency which the control loop should not attempt to reject. The output capacitor is chosen to be large to keep this low-frequency ripple of the output-voltage small.

18.4.2.2 Three-phase

The three-phase boost topology, *Figure 18.46*, is very similar to a standard three-phase inverter, *Figure 18.32*. PWM of the inverter switches can be used to generate three voltages, V'_A, V'_B, V'_C similar in phase and magnitude to V_A, V_B, V_C once a voltage has been established on the d.c. side. (Precharge of the capacitor through the diodes of the circuit is problematic and needs some form of in-rush protection.)

Power flow through the Boost converter is controlled in the same manner as a standard synchronous machine. The phase difference (or load angle), δ, can be set by the PWM system and used to control the real power flow,
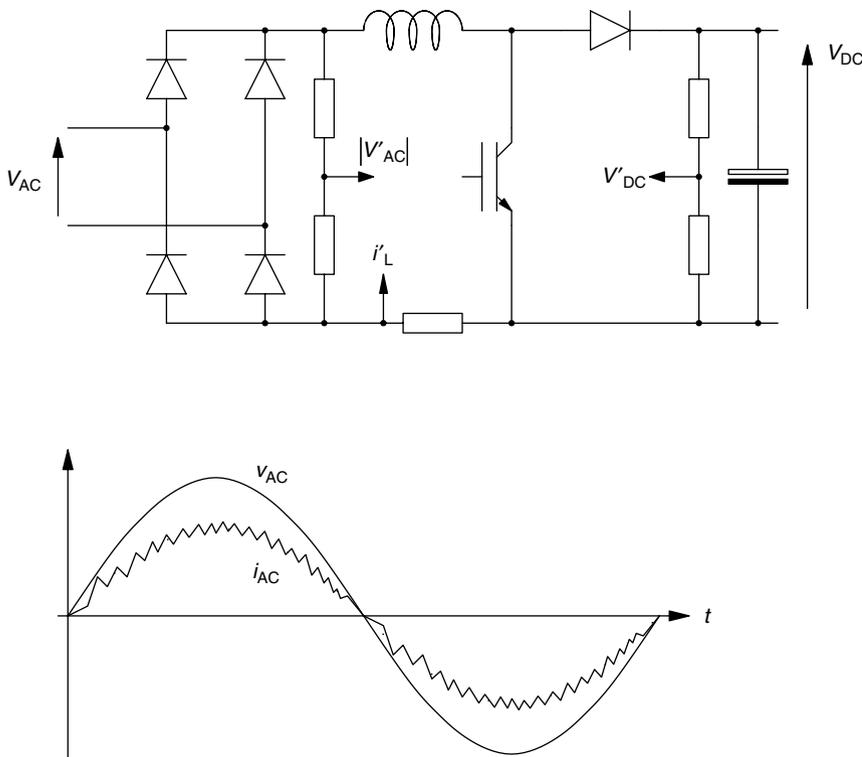
Figure 18.43 Single-phase Boost a.c./d.c. converter including its measurement points and example waveforms
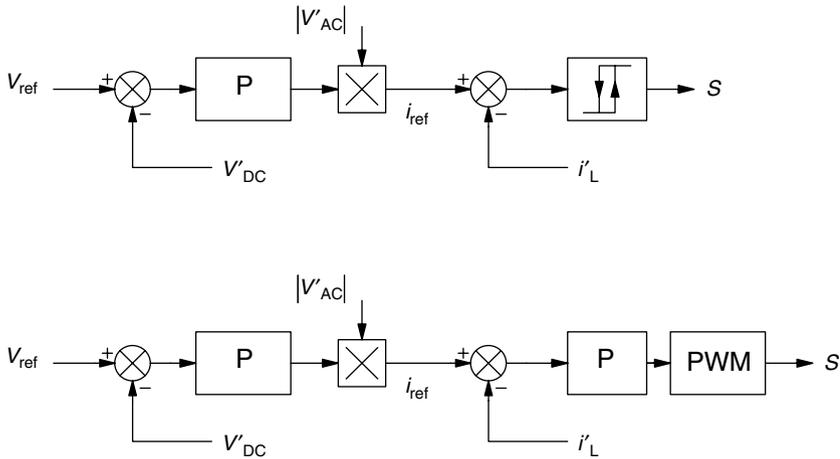
Figure 18.44   Hysteresis and PWM methods of current control

Figure 18.47. The voltage magnitude could also be used to control the reactive power flow. The Boost converter is able to operate in all four quadrants of the $S = P + jQ$ plane. This is useful for regenerative systems since power can be returned to the a.c. system. It is employed in some drive systems where sustained regeneration warrants the extra cost of this converter over a diode rectifier plus 'dump' resistor (Sections 19.3.4.1 'Voltage Source Inverters' and
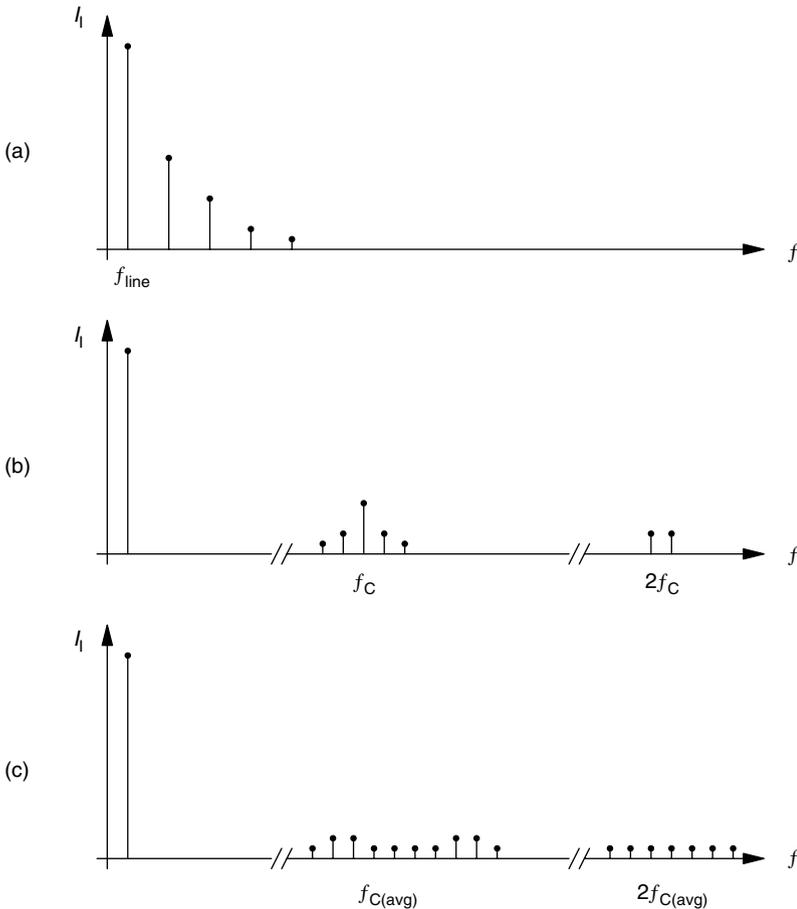
Figure 18.45   Frequency spectra of (a) diode rectifier, (b) PWM controlled a.c./d.c. converter and (c) hysteresis controlled a.c./d.c. converter
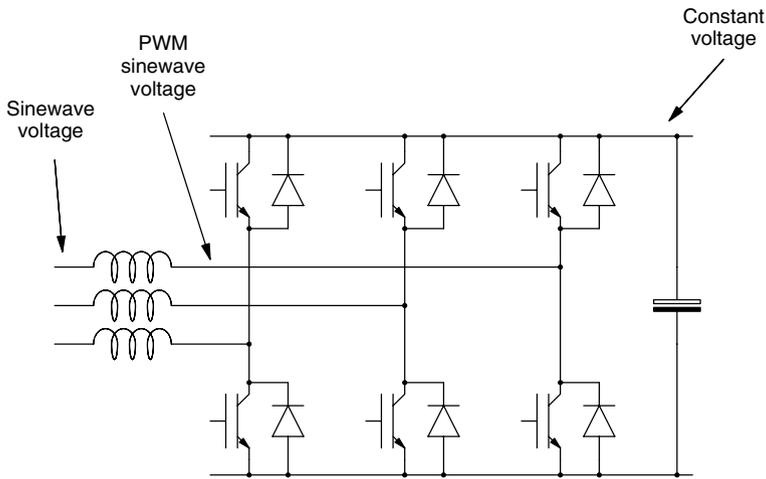
Figure 18.46   Three-phase boost a.c./d.c. converter
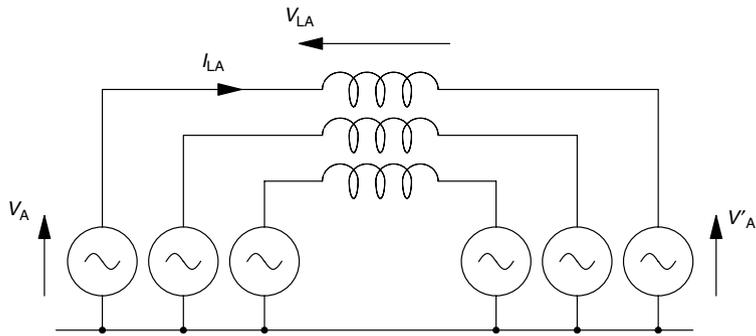
Rectifier mode
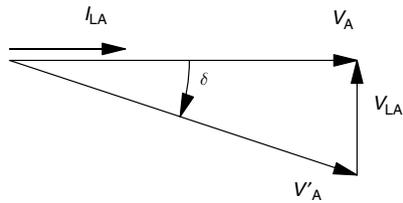
Inverter mode
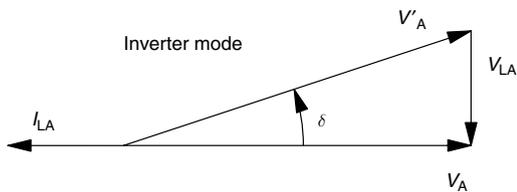
Figure 18.47   Bi-directional power flow controlled through phase-shift of voltage

19.4.2.4 'Four Quadrant Operation'). It is common to implement current control in this class of converter and separately control the in-phase (real power) and in-quadrature (reactive power) components of current. This might well be performed in the *dq*-domain following Clark and Park transforms of the variables.

18.5 A.c./a.c. conversion

There are circuits that will convert directly from one a.c. frequency and voltage to another a.c. frequency and voltage. These are known as cyclo-converters and matrix converters. However, they are not as attractive as might at first appear because they use a greater number of semiconductor switches than indirect methods of a.c./a.c. conversion.

18.5.1 A.c. voltage regulator

Where control of voltage amplitude only is required, then the techniques of phase-angle control described in Section 18.4.1 can be used. *Figure 18.48* shows a pair of thyristors in anti-parallel used as a phase-angle controlled switch to regulate the voltage applied to a single-phase load. Conduction of each thyristor can be initiated at any point in the appropriate half-cycle. With an inductive load, conduction will continue part way into the following half-cycle. In low power applications, such as incandescent lamp dimmers and a.c. commutator motors in domestic white-goods, a TRIAC would replace the pair of thyristors. Three-phase versions of this circuit are sometimes used as soft-start circuits for induction machines as discussed in Section 19.3.5.1 'Soft-Starter/Voltage-Regulator'.
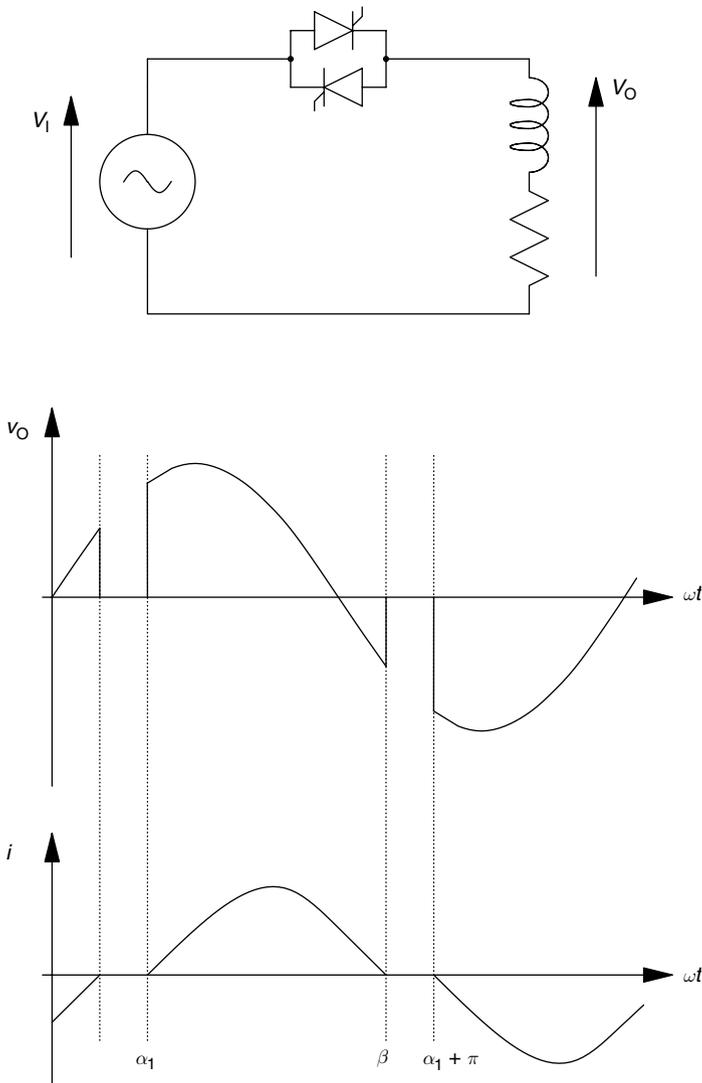
Figure 18.48 Phase-angle controlled a.c. voltage regulator

18.5.2 Direct frequency converter

18.5.2.1 Cyclo-converter

The cyclo-converter is able to provide direct a.c. to a.c. transformation with control over both the output voltage magnitude and output frequency. It uses phase-angle-controlled bridges to synthesise voltages. The most common form is the three-phase to three-phase converter of *Figure 18.49*. Each output requires two three-phase thyristor bridges of the same form as the rectifiers of *Figure 18.40*. One bridge is used to synthesise positive voltages at the output; the other is connected in reverse and synthesises negative voltages. The phase-angles of the bridges are gradually altered to give an approximately sinusoidal variation of the voltage at the output. Both the output voltage and the input current are rich in harmonics and some form of filtering is normally required. The frequency of the output voltage is constrained to less than about 1/3 of the input frequency by the allowable distortion of the input current. To prevent shoot-through paths between the phases while thyristors are commutating, the input phases are isolated using transformers. Cyclo-converters are employed for very high power, low speed machine drives where the complexity of the circuit is less of a problem and where line-frequency thyristors are the only viable device (Section 19.3.5.2 'Cycloconverter'). Cylco-converters are able to transfer power in either direction and can form the basis of a four-quadrant drive (c.f. the choppers of Section 18.2.1.1).

18.5.2.2 Matrix converter

The matrix converter performs a similar function to the cyclo-converter but employs semiconductors that can be commutated off (in contrast to thyristors). The switches are operated at high frequency to synthesise high-quality waveforms free of low-order harmonics. In its three-phase to three-phase form, *Figure 18.50*, the matrix converter requires 9 bi-directional switches to provide connections between every input phase and every output phase. There are no suitable intrinsically bi-directional semiconductor switches so each switch is made up of two uni-directional semiconductor switches. There are several possible ways to configure the uni-directional switches to achieve this. Like the cyclo-converter, the matrix converter is able to transfer power in either direction and can form the basis of a four-quadrant drive.

The circuit is normally placed between a voltage–source input and a current–sink (or inductive) output. It is imperative that there is always a path for each output current to flow and that there is never a short circuit path between two input connections. Given the finite switching times of devices this requires care. There are commutation sequences that meet these constraints provided that the two uni-directional halves of the switches are individually controlled in keeping with the prevailing voltages and currents.

18.5.3 Indirect frequency converter

We can convert a.c. to a.c. via d.c. using a pair of converters and a d.c.-link, *Figure 18.51*. The a.c. to d.c. converter will require 6 semiconductor switches and the d.c. to a.c. converter a further 6 switches. The total, 12 switches, is less than the 18 (uni-directional) switches required for the matrix converter or the 36 required for the cyclo-converter. However, the indirect conversion requires an energy storage component in the d.c.-link.
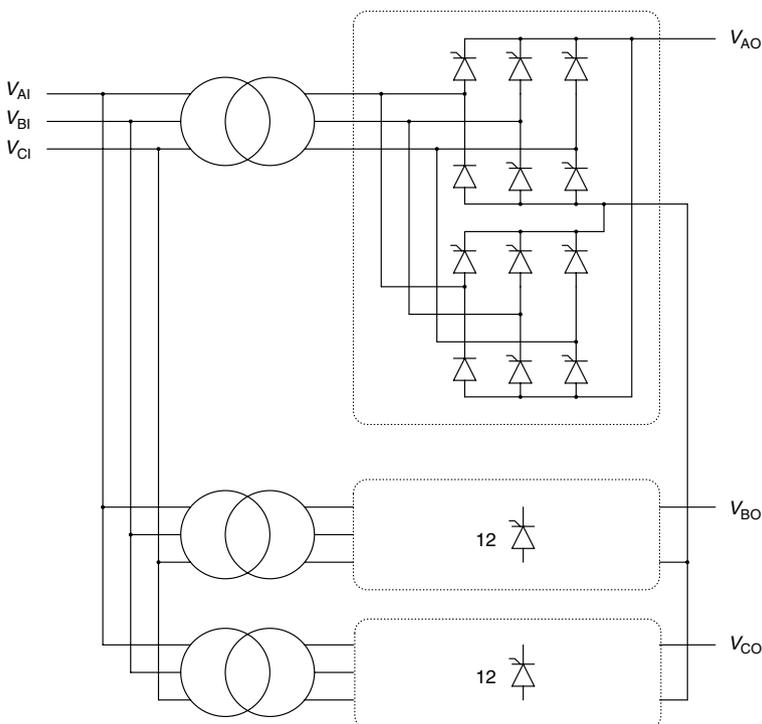
Figure 18.49 A three-phase to three-phase cyclo-converter
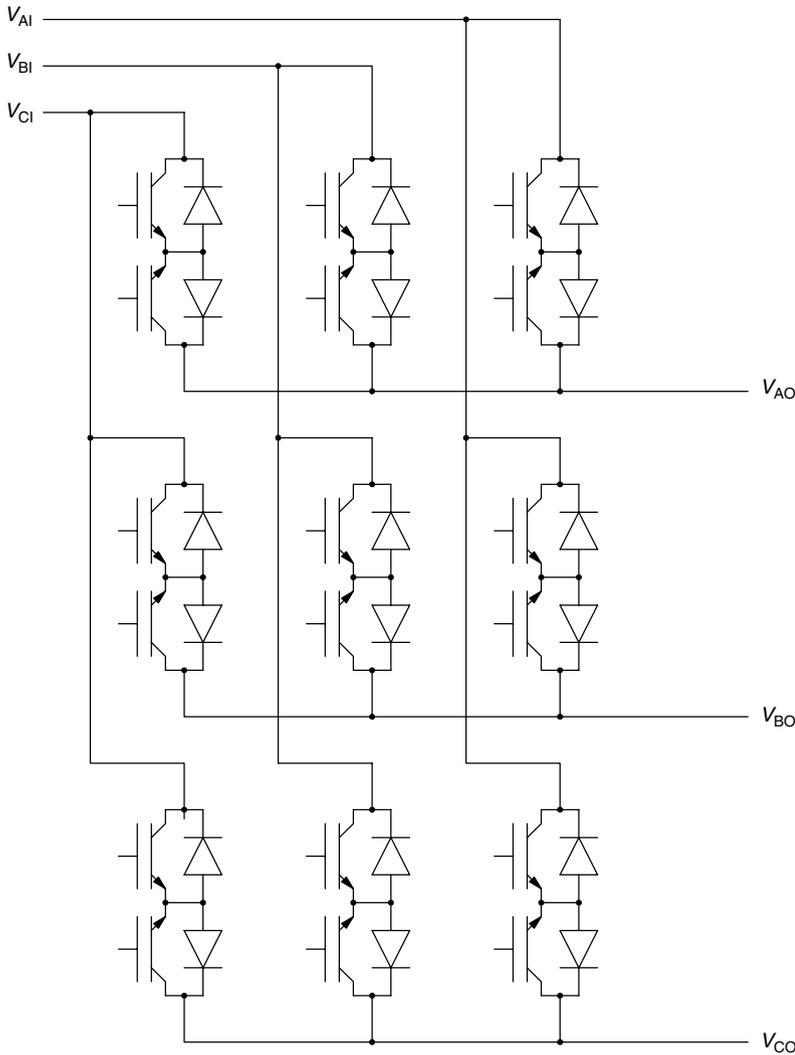
Figure 18.50   A three-phase to three-phase matrix converter

The inverter on the output-side can naturally transfer power in either direction. The rectifier on the input-side could be diode based on *Figure 18.37* and therefore capable of only uni-directional power flow. This would suit a two-quadrant drive system. If a four-quadrant drive system is required then a bi-directional rectifier based on *Figure 18.46* should be used. There is, of course, a cost penalty in using the more complex bi-directional circuit. If the drive system is re-generative for only brief periods (short periods of deceleration for instance) then a uni-directional rectifier

Figure 18.51   Indirect frequency conversion using a d.c.-link

and a resistive energy dump might be used as discussed in Section 19.4.2.4 'Four Quadrant Operation'.

The most common form of indirect conversion is using voltage source converters and a capacitive link. The d.c.-link capacitor is both a strength and a weakness of this circuit. It must exist to provide the short-term (switching cycle) energy storage to attenuate voltage ripple. In practice the capacitor is much larger than this and can provide sufficient energy storage to enable a system to operate through a momentary loss of supply. Its energy storage can also prevent low frequency variation of power flow on one side feeding through to the other (provided that the controller is so designed). This is useful for avoiding 'flicker' problems, i.e. voltage disturbances at a point of common coupling that would cause flicker of light output at frequencies (circa 12 Hz) that are irritating to the human eye.

The weakness of the d.c.-link capacitor is that it will normally be an electrolytic capacitor that has a relatively short

lifetime. The lifetime is degraded at elevated temperatures and this can be a severe limitation in some applications.

18.6 Resonant techniques

Section 18.1.2 discussed the power dissipation in a semiconductor switch when a transition is made between on- and off-states. It was shown that in commutating the current in an inductive load, the switch is subjected to a coincidence of voltage drop and current flow and as a consequence the instantaneous power dissipation is high. Because there is a certain energy loss per commutation, the operating frequency (commutations per second) must be limited. However, there are ways to break this limit. The switching trajectory has to be modified so that either the current or the voltage or both are held at zero while commutation is performed. This is illustrated in *Figure 18.52*. The hard-switched trajectory shown is idealised. The trajectory will be modified, and energy loss increased, both by diode recovery at turn-on and voltage overshoot at turn-off.

There are two approaches to modifying the switching trajectory. One is to add a snubber circuit to the switch and control the rise of current at turn-on and rise of voltage at turn-off. Snubbers are discussed in Section 17.2.1 and several circuits are described.[6,3] The other approach is to modify the load circuit so that the load seen by the switch naturally has periods of zero voltage or zero current that present opportunities to turn on or off without incurring power dissipation. This second method covers techniques known as soft-switching and resonant power converters. As will be seen in this section, additional current flow is necessary to ensure that the correct switching conditions are achieved. Thus, there is a penalty to be paid in conduction losses for the reduction in switching losses.
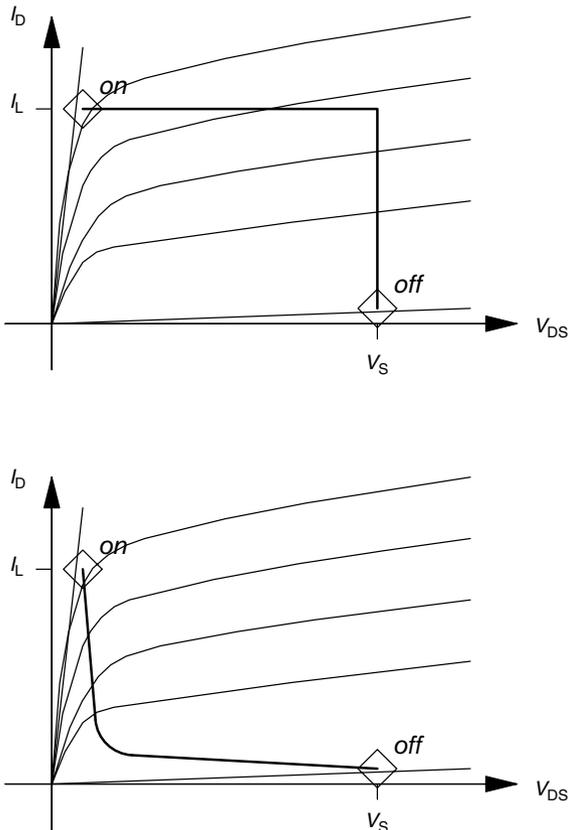
Two examples will be given here of the resonant circuit technique. The technique has been applied to almost every power converter circuit configuration.

18.6.1 Quasi-resonant SMPS

The term quasi-resonant describes a circuit that has one stable condition (one of either on- or off-states) and a resonant condition initiated when the switch changes state. The circuit is operated such that one cycle of resonant action occurs and then the circuit resumes its stable state.

18.6.1.1 Zero-current switched Buck SMPS

The circuit of *Figure 18.53* is a standard Buck SMPS with a resonant inductor–capacitor pair, $L_R C_R$, and an extra diode added. The circuit has a stable state when the transistor is off and the current in L_O flows through main diode D. For the purpose of the following analysis, the current in L_O is assumed to be constant and equal to the output current, I_O. A resonant cycle is initiated by turning the transistor on. As shown in *Figure 18.54*, this creates a pulse of voltage across C_R that is applied to the LC filter at the output. The duration of the pulse is fixed by the resonant frequency of $L_R C_R$, but the period between the pulses can be controlled by setting the off-time of the transistor. Thus the output voltage can be regulated.

The stages of operation are:

(I) The transistor is off and I_O flows in D. This state is stable.
(II) The transistor is turned on and the input voltage is imposed across L_R. As a consequence i_{LR} rises linearly. D stays in conduction (and v_{CR} is held close to zero) because i_{LR} is less than I_O. This period lasts until $i_{LR} = I_O$.
(III) D falls out of conduction and $L_R C_R$ form a resonant circuit governed by:

$$V_i = v_{C_r} + L_r \frac{d}{dt}(i_{C_r} + I_O)$$
$$= v_{C_r} + L_r C_r \frac{d^2 v_{C_r}}{dt^2} \qquad (18.44)$$

with initial conditions of $i_{LR} = I_O$ and $v_{CR} = 0$. Solving this differential equation yields:

$$I_{L_R} = I_O + \frac{V_I}{\omega_R L_R} \sin(\omega_R t)$$
$$V_{C_R} = V_I (1 - \cos(\omega_R t)) \qquad (18.45)$$

where $\omega_R = \frac{1}{\sqrt{L_R C_R}}$

It is important that i_{LR} swings negative, period IIIb. When this happens, i_{LR} is carried by D_R and the transistor carries no current. The transistor can be switched off any time during period IIIb without incurring power dissipation. The circuit must be designed

Figure 18.52 Hard-switched and soft-switched trajectories on the voltage/current plane
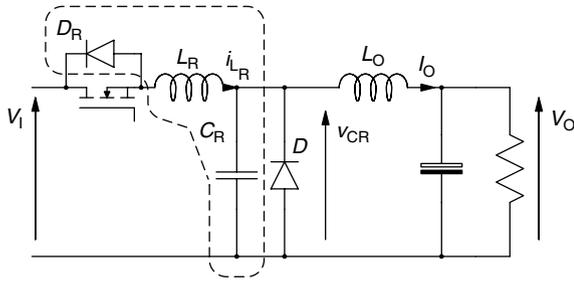
Figure 18.53 Zero-current switched Buck SMPS
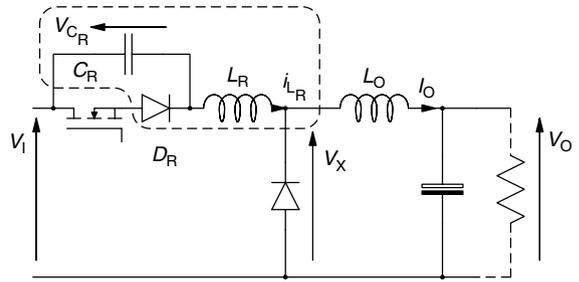
Figure 18.55 Zero-voltage switched Buck SMPS

transistor on, and resonance is initiated by turning the transistor off. As shown in *Figure 18.56*, this produces a dip in the voltage applied to the output LC filter. The output voltage can be regulated by controlling the on-time of the switch.

The stages of operation are:

(I) The transistor is on and I_O flows through the transistors, D_R and L_R. This state is stable.

(II) The transistor is turned off and the current I_O ($=i_{LR}$) is diverted into C_R. C_R holds the voltage across the transistor low while it switches. The diversion of I_O causes v_{CR} to rises linearly. This continues until $v_{CR} = V_I$ at which point the main diode D becomes forward biased and provides an extra current path.

(III) With D in conduction, i_{LR} is free to change and $L_R C_R$ form a resonant circuit governed by:

$$V_i = v_{C_r} + L_r C_r \frac{d^2 v_{C_r}}{dt^2} \qquad (18.47) \Leftarrow$$

with initial conditions of $i_{LR} = I_O$ and $v_{CR} = V_I$.
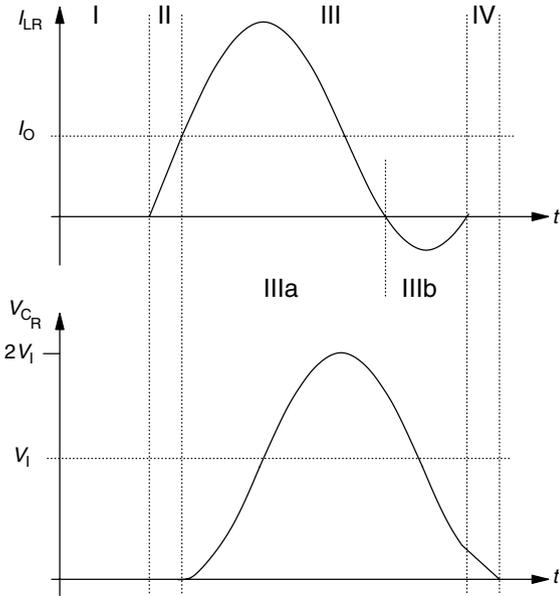
Figure 18.54 Waveforms of the resonant components of a ZCS QR Buck SMPS

such that $\frac{V_I}{\omega_R L_R}$ safely exceeds I_O so that the zero-voltage condition is ensured. This can lead to substantial extra current flow and raised conduction loss.

Period III ends when the i_{LR} rises again to zero but is blocked from becoming positive because the transistor is off.

(IV) When period III ends there is residual charge on C_R that is discharged (linearly) by the continued flow of I_O. This period ends when v_{CR} reaches zero and D is brought into conduction. The circuit then re-enters the stable state I.

If period IV is short then the average voltage during period III is V_I and the output voltage is given by:

$$\frac{V_O}{V_I} \approx \frac{t_R}{T} \approx \frac{2\pi f}{\omega_R} \qquad (18.46) \Leftarrow$$

18.6.1.2 Zero-voltage switched Buck SMPS

The zero-voltage switched Buck SMPS, *Figure 18.55* is the dual of the zero-current switched circuit. Its stable state is with the
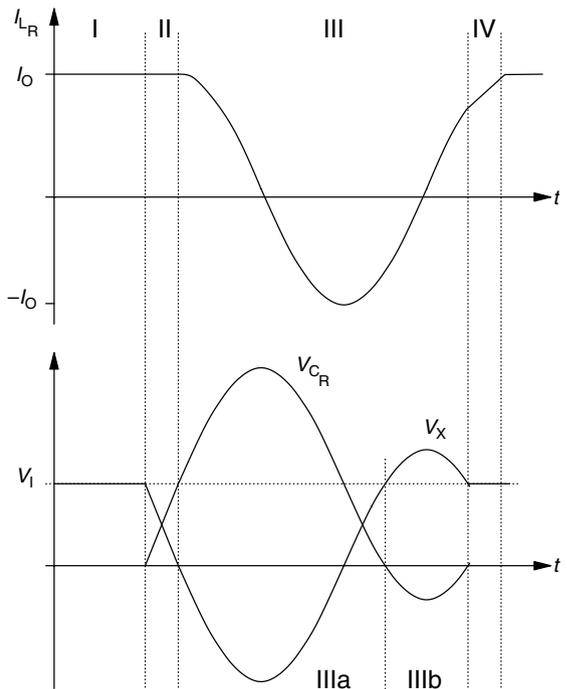
Figure 18.56 Waveforms of the resonant components of a ZVS QR Buck SMPS

Solving this differential equation yields:

$$I_{LR} = I_O \cos(\omega_R t)$$
$$V_{C_R} = V_I + \frac{I_O}{\omega_R C_R}\sin(\omega_r t) \qquad (18.48)$$

It is important that v_{CR} swings negative, period IIIb. When this happens, D_R is reverse biased and the transistor no longer has to support voltage. The transistor can be switched on at any time during period IIIb without incurring power dissipation. The circuit must be designed such that $\frac{I_O}{\omega_R C_R}$ safely exceeds V_I so that the zero-voltage condition is ensured. Period III ends when the v_{LR} rises again to zero but is prevented from becoming positive because the transistor is on.

(IV) When period III ends, the current i_{LR} is less than I_O. L_R has the input voltage imposed across it (because D must still be in conduction to carry the short fall in I_O) and so the current rises. This period ends when i_{LR} reaches I_O and D is released from conduction. The circuit then re-enters the stable state I.

18.6.2 Resonant SMPS

The difference between quasi-resonant and resonant circuits is not distinct. The terms are used here to differentiate between circuits that are operated at or slightly off resonant frequency with essentially continuous resonant action and those of the previous section in which the resonant action is paused for a period.

Figure 18.57 is an example of a half-bridge used to excite a series combination of inductance and capacitance. A load, comprising a full-wave rectifier and reservoir capacitor, is connected in series with the resonant circuit. This is known as a series-loaded resonant converter.

The parallel-loaded variant (that is, a load connected in parallel with the capacitor) is shown in *Figure 18.58*. This circuit also incorporates transformer isolation.

There are various operating modes of these circuits depending on the ratio of the resonant frequency to the switching frequency of the switches. The modes are defined by whether more than one, less than one or less than a half of a resonant cycle is completed between each commutation of the switches.[3] The output of the circuit is controlled by varying the operating frequency. In the case of the series-loaded circuit this varies the current delivered to the output filter; in the case of the parallel-loaded circuit, this varies the voltage applied to the output filter.
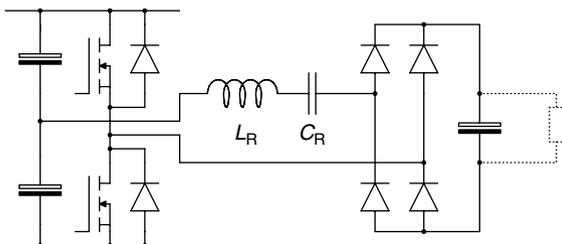
Figure 18.57 A series-loaded resonant SMPS
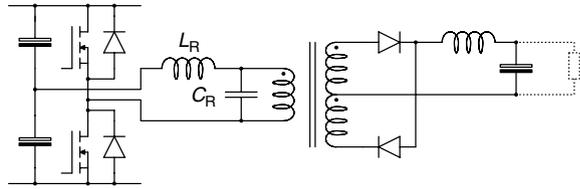
Figure 18.58 A transformer isolated, parallel-loaded resonant SMPS

An advantage of these circuits is that the parasitic capacitance of the semiconductors can be utilised in the normal operation of the circuit and may be supplemented with additional parallel capacitance. Thus, the voltages across the devices have limited rates-of-change.

Many forms of resonant SMPS exist. In addition, circuits without the full-wave rectifier are used to supply high frequency a.c. for applications such as induction heating furnaces.

18.7 Modular systems

For some applications power converters are built from modules. There are several reasons why this might be done.

First, device ratings are limited and for power converters of very high rating no single device can match the required rating. This is sometimes solved by series or parallel connection of devices to form composite switches (often known as valves in the power industry). An alternative is to form lower rated power converter modules from individual
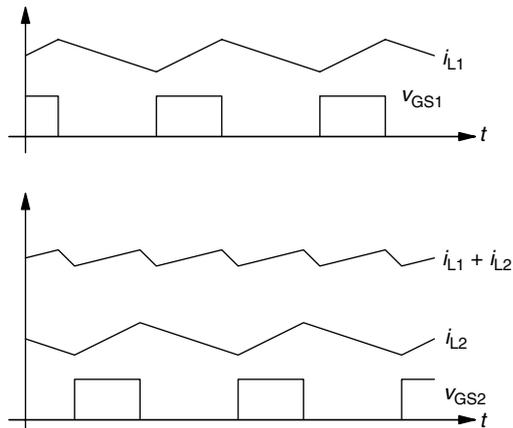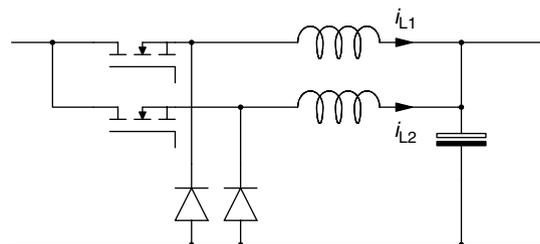
Figure 18.59 A pair of interleaved Buck SMPS showing a reduction of amplitude and increase in the effective frequency of the current ripple
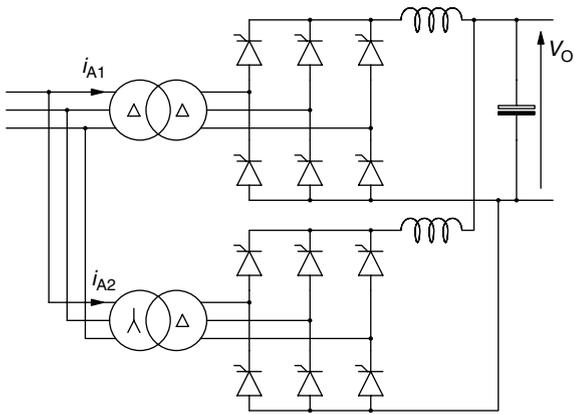
Figure 18.60   A 12-pulse rectifier
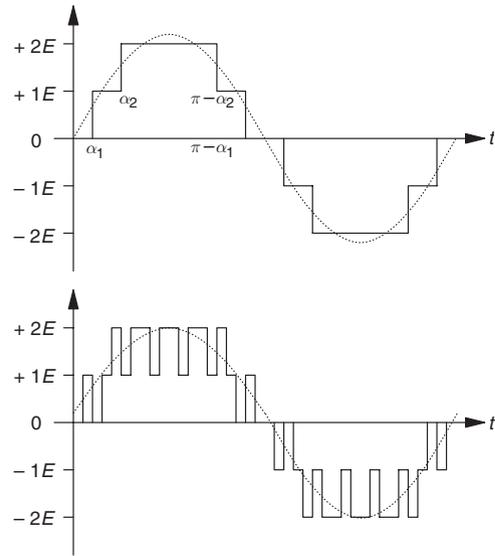
Figure 18.61   5-level staircase and PWM waveforms
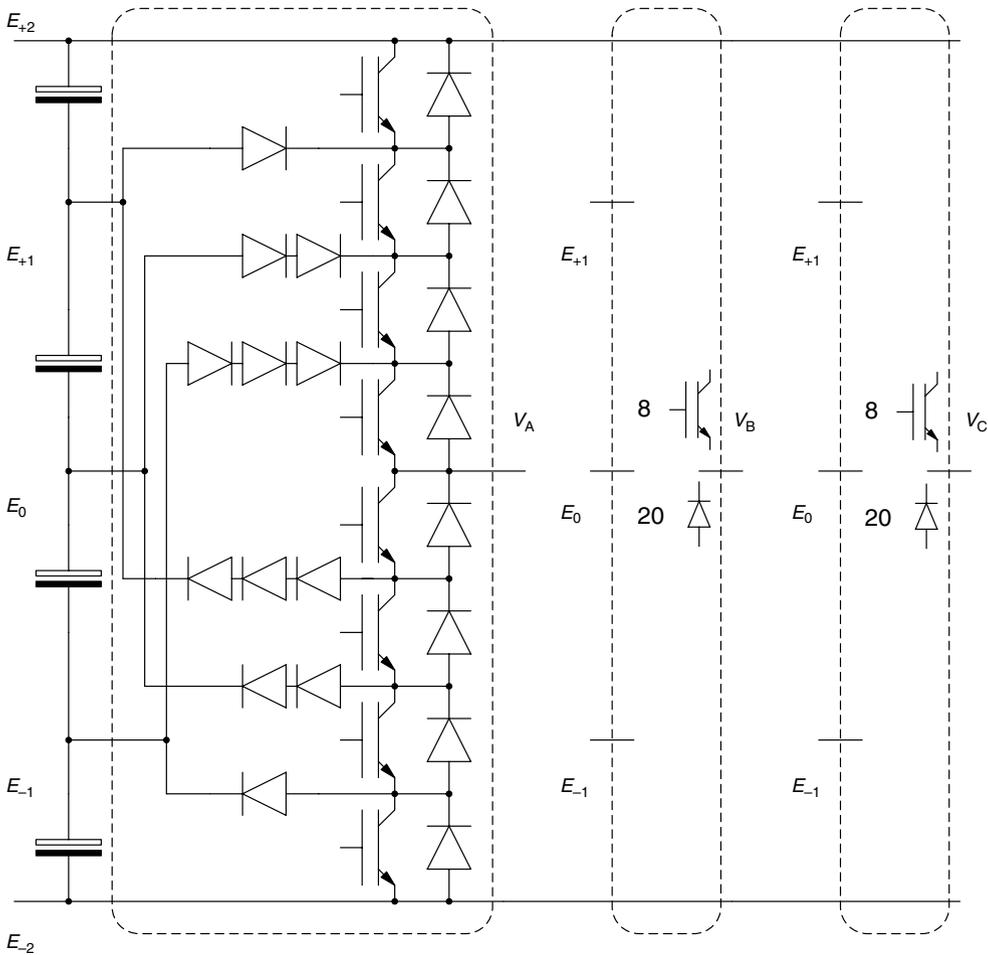
Figure 18.62   A 5-level multi-point clamped inverter
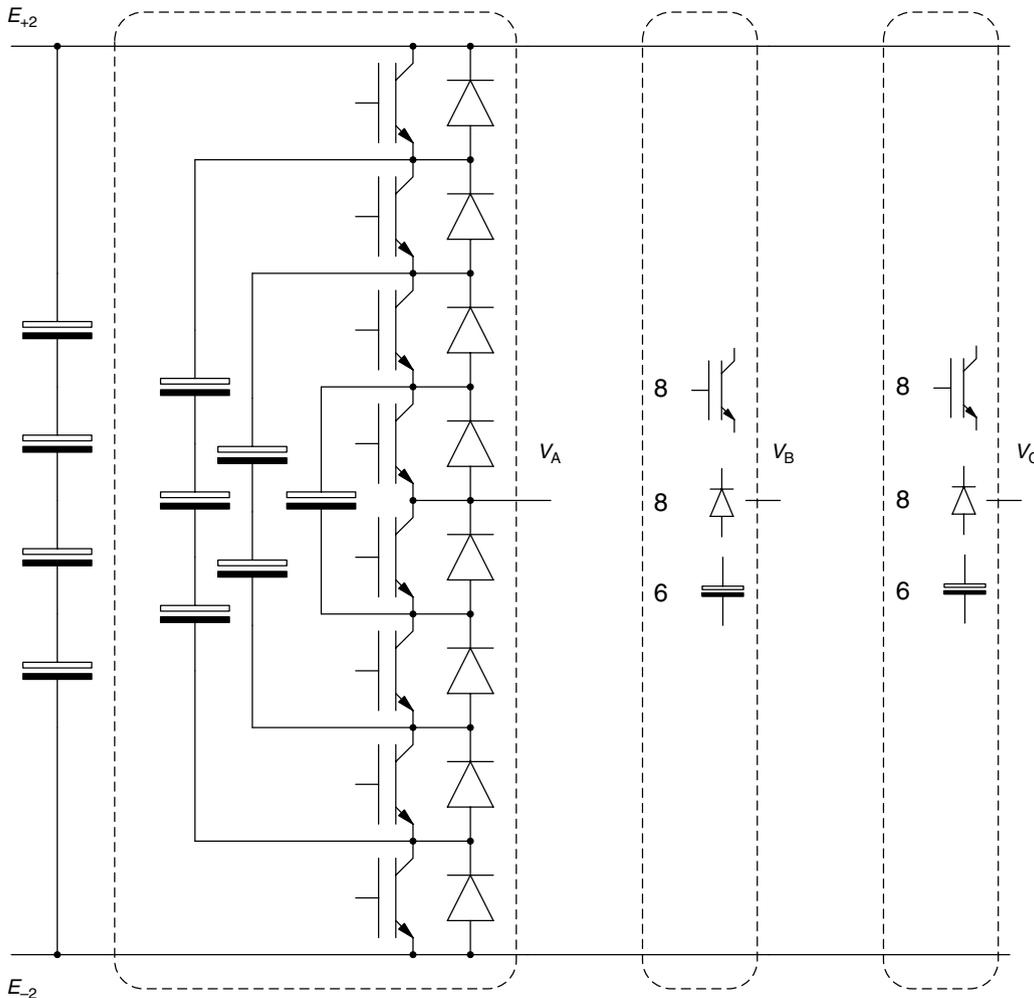
Figure 18.63 A 5-level nested cell inverter

switches and then connect the modules in series or parallel to achieve the desired rating.

Second, switching power loss limits the maximum frequency at which a power converter may operate. If several modules are operated with interleaved switching, then the overall circuit has an effective switching frequency equal to the switching frequency of each individual module multiplied by the number of modules. Each module is rated for a fraction of the voltage (series connection) or fraction of the current (parallel connection).

Third, in applications where reliability is a major concern, redundancy may be provided through modular construction with a greater number of modules than necessary to meet the power rating. The 'more-electric aircraft' and 'more-electric ship' are example application areas.

Some application areas combine all of three reasons. The STATCOM (a d.c./a.c. converter used for reactive power support) presently being commissioned by Alstom for National Grid PLC in the UK is a modular, chain-cell design. In this case:

(i) the voltage ratings are such that no single switch is suitable,

(ii) the switching frequency of high-rating GTO thyristors is low and good waveform quality can only be achieved through independent operation of multiple devices and

(iii) the availability requirement specified by the user is such that the equipment must continue to operate after the failure of one or possibly two devices and, therefore, each chain must contain redundant elements.

18.7.1 Interleaved SMPS

There is a strong desire in SMPS design to reduce output voltage ripple and input current ripple (especially in mains connected equipment subject to EMC constraints). *Figure 18.59* shows an example of parallel connected output stages with interleaved operation of the switches. It can be seen that the resultant current ripple is at twice the frequency of operation of the switches and that each switch has processed half of the current. Viewed in the frequency domain, we would see ripple current components at all of the even multiples of the switching frequency, whereas those at odd multiples created by one module will have been cancelled by those created (in anti-phase) by the other module. The same

principle was used in the single-phase d.c./a.c. converter of Section 18.3.1 in which the two halves of the bridge were operated with phase-shifted carriers.

This idea can be extended to series connection of modules and to any number of modules. It can be applied to the input connection, output connection or both. In general, an n-module system has an effective switching rate (ripple frequency) of $n f_s$. In all cases it is important to match components and operating conditions in the modules in order to achieve the desired cancellation of ripple components.

18.7.2 Multi-pulse rectifiers

The diode and thyristor rectifiers of Section 18.4.1 were seen to create distorted a.c.-side currents with harmonic distortion of order $6k \pm 1$ for three-phase systems. This situation can be improved by operating rectifier modules with phase-shifts between them such that some of the harmonics created by one module are cancelled by those of another. These rectifiers are described by their pulse number. The standard rectifier creates a voltage (or current) waveform on the d.c.-side with 6 pulses per cycle. Adding a second unit with appropriate phase shift creates 12 pulses. Any number of 6-pulse modules can be combined to produce higher pulse number rectifiers. Combining n modules creates a $6n$-pulse rectifier that generates a.c.-side harmonics of order $6nk \pm 1$. That is, the first $(n-1)$ pairs of characteristic harmonics (and their multiples) are cancelled.

Figure 18.60 shows an example of a 12-pulse rectifier with parallel connection on the d.c.-side. One 6-pulse module is supplied through a delta–delta transformer (with no phase shift) and the second is supplied through a star–delta trans-former providing 30° of phase advance. The thyristors of the second module are fired ahead of those of the first module by a time-shift equivalent to 30° of a mains cycle. This gives a 12-pulse pattern on the d.c.-side. The current drawn by the second module is also time-shifted forward but the fundamental is re-aligned with the first module by the 30° phase-shift of the transformer. Each harmonic is affected differently by the time-shift created by the thyristor firing and the phase-shift (which is phase-sequence dependent) of the transformer. For example, the 5th and 7th harmonics created by the two modules are in anti-phase and cancel whereas the 11th and 13th harmonics are in phase and add.

Zig-zag or differential delta transformers can be used to give the small phase-shifts necessary to construct high pulse-number rectifiers (n increments of $60°/n$ for a $6n$-pulse system).[5]

18.7.3 Multi-level inverters

The multi-pulse techniques of Section 18.7.2 have also been used for inverters and reactive power compensators. However, the complexity and bulk of the transformer system is a considerable disadvantage. Instead, inverters can be constructed in which the output voltages can be synthesised by switching between many voltage levels rather than the two levels of the circuit in *Figure 18.32*. In high-power inverters, the switches are operated at line frequency and the waveform synthesised as a staircase, *Figure 18.61*. In medium-power inverters, PWM or SVM can be used to operate the switches at high frequency. In the line-frequency-switched case, the angle of each transition can be optimised to meet harmonic distortion criteria.
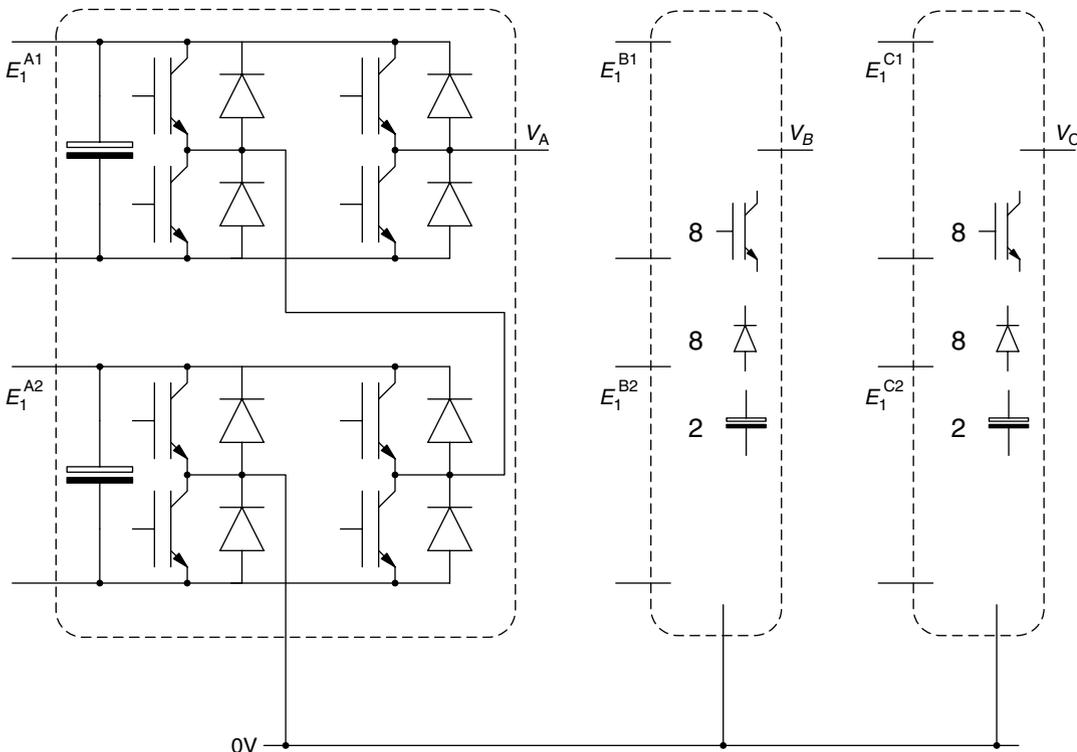
Figure 18.64   A 5-level chain cell inverter

There are several types of circuit for implementing multilevel inverters. Three examples of 5-level inverters are shown in *Figure 18.62*, *Figure 18.63* and *Figure 18.64*. Note that each circuit uses 8 transistors per phase and each transistor has a voltage rating of one level and a current rating of the full phase current. The differences between the circuits lie in how the numbers of other components (diodes and capacitors) increase with the number of levels.

The multi-point clamped circuit, *Figure 18.62*, has the advantage that the capacitor chain is shared between the three phases. This reduces the ripple in the capacitors (for balanced conditions) and allows smaller volume capacitors to be used than with the other implementations. Its principal disadvantage is the number of clamping diodes required (and that some of these must be series connections to span multiple voltage levels). Charge drawn from each capacitor must be managed to ensure that the capacitors remain balanced. To some extent this can be achieved in SVM by utilising redundant states. This cannot be achieved under all conditions (where suitable states do not exist) and auxiliary balancing circuits are required.

The nested-cell circuit, *Figure 18.63*, (also known as the flying capacitor inverter) avoids high voltage clamp diodes but requires capacitors to set the voltage levels. Operation of the circuit must be managed to ensure that the correct voltage is maintained on each capacitor. Only one of the capacitor chains is common to all phases. The volume of capacitance required is greater than for the other designs.

The chain-cell converter, *Figure 18.64*, avoids both a larger number of diodes or a large volume of capacitance. It is the only circuit in which the component numbers increase linearly with the number of modules. However, each module requires an isolated d.c.-link. This makes the circuit difficult to apply where a.c./d.c./a.c. conversion is required, for instance, in a drive system. The chain-cell inverter is suitable for floating (i.e. supply-less) applications. It has been used for reactive power compensation as mentioned in the introduction to this section.

18.8   Further reading

This chapter has given a flavour of the opportunities afforded by power electronics in power conversion. It has also introduced some of the analysis necessary for design. However, there are several topics that need further treatment before practical design could be attempted.

In all but the simplest circuits, the semiconductor devices need to be operated in the correct environment. Texts such as[6,3] give details of the gate drive circuits (including electrical isolation of signal and power), protection against overvoltage and over-current, snubber circuits and thermal management. Power electronic circuits put unusual voltage and current stresses on passive components too and so these components need to be chosen with care.

As indicated in the main text, there is a huge variety of SMPS circuits and almost any combination of voltage transfer characteristics, isolation and resonant action can be found.[2,3,6] There is a similarly large variety of single-phase a.c./d.c. converter circuits and a good review of these has been provided by[1]. This review also discusses the usefulness of circuits that fall short of perfectly sinusoidal current but still meet distortion standards. Control of SMPS is a large subject in itself.[3]

Line-frequency-switched converters can cause serious distortion to a.c. systems. The severity of the distortion needs to be analysed and harmonic mitigation will often be required.[5]

Control of power converters with a 3-phase a.c. connection is often best achieved in a rotating co-ordinate system in which the sinusoidal variation of the signals is removed. This is discussed in several texts in terms of control of a.c. machines, for instance.[4]

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