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Lockheed F-22 Raptor

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32.1 F-22 Role and Mission

The F-22 will replace the F-15 as the U.S. Air Force's next generation air superiority fighter. With a first-look, first-shoot, first-kill capability it will maintain U.S. air supremacy in air-to-air and air-to-ground roles in the 21st century. It will deploy a wide mix of missiles and stand-off weapons which, under the guidance of the Integrated Avionics System (IAS), will provide the pilot with robust lethality and mission survivability.

32.2 IAS Hierarchical Functional Design

Behind this first-look, first-kill capability is the F-22's ability to establish superior situational awareness concerning target detection, location, identification, and lethality. The IAS provides the pilot situational awareness well Beyond Visual Range (BVR). Data fusion from multiple sensors is used to achieve long-range detection, high confidence BVR-Identification (BVRID) and highly accurate target tracking for BVR weapons employment and/or threat avoidance. The IAS directly contributes to increased survivability by providing threat warning and countermeasures against threat systems.

This first-look, first-kill requirement depends on the ability to collect data from multiple onboard sensors, to develop a highly accurate track file on enemy targets, and to do so before the F-22 is detected by enemy sensors. Each target track file is continually and automatically updated without pilot intervention. Targets receive increasingly tighter tracking accuracies as they penetrate a series of tactical engagement boundaries surrounding the F-22 as shown in Figure 32.1. From outermost inward, these "globes" are called (1) Situation Awareness Initial Track/ID, (2) Engage/Avoid Decision, (3) BVRID Initial AMRAAM Launch, (4) Initial Threat Missile Launch, and (5) Threat Missile Lethal Envelope. The globe boundary concept, inherent in the tactical software design, supports both (1) efficient sensor usage and (2) automated sensor tasking. It provides the pilot adequate time to make tactical decisions (such as engage, avoid, commit weapons, or expend countermeasures) instead of controlling sensors.

All multisensor information must be fused or correlated into a consistent, valid, integrated track file. This is done automatically by the sensor track fusion algorithms and the "smart" sensor-tasking

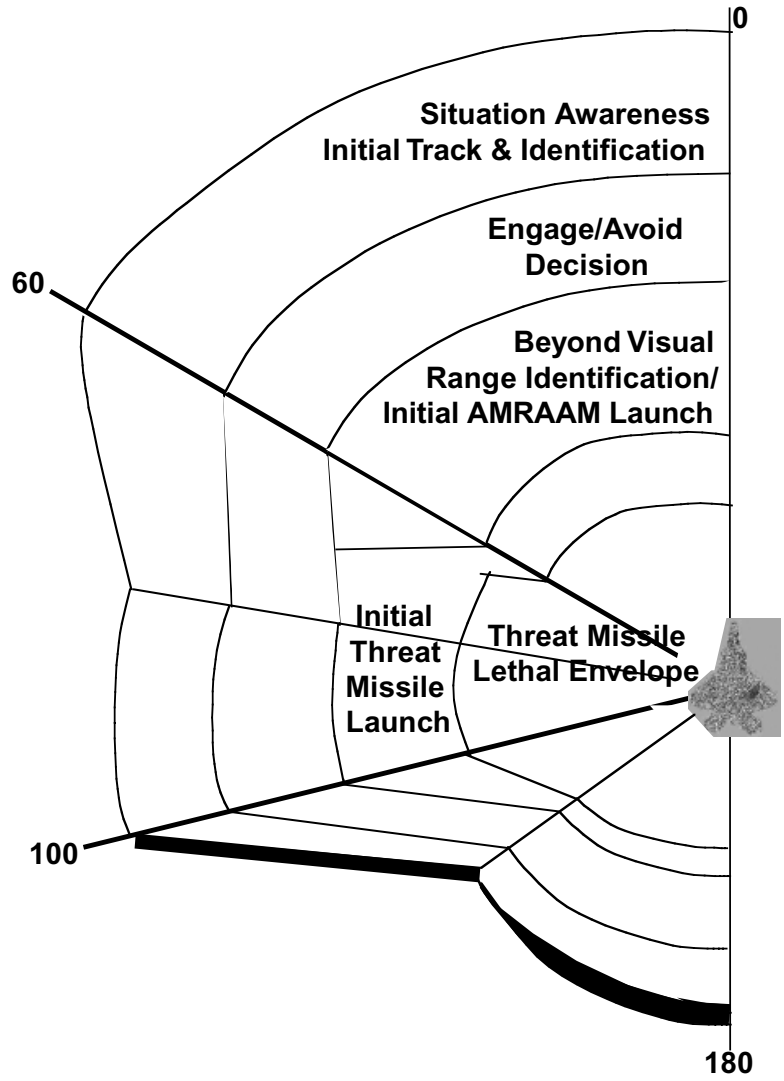

FIGURE 32.1 F-22 globe boundaries.

algorithms which are tailored to support each globe boundary's requirements. The integrated track file is then presented to the pilot on the integrated offensive, defensive, and area-wide situational awareness tactical displays.

Mission Software (MS/W) serves as the central controller of IAS operations, interfacing to all sensors, processors, pilot controls, and displays. It manages, coordinates, and supports the overall integrated capability to search, detect, track, identify, employ weapons, and expend countermeasures against airborne or ground threats. MS/W accomplishes this through a hierarchical functional tree consisting of three principle levels: the *integrating functions* level, the *decision-aiding functions* level, and the *mission functions* level (see Figure 32.2).

At the first level, the integrating functions manage and control the various onboard sensors. Sensor data are fused and correlated with navigation data to form integrated airborne and ground track files. This information is then sent to the second level of processing: the decision-aiding functions level.

At the second level, decision-aiding functions do critical assessments of the overall offensive and defensive tactical situation. Three key assessments are performed on the integrated track files received.

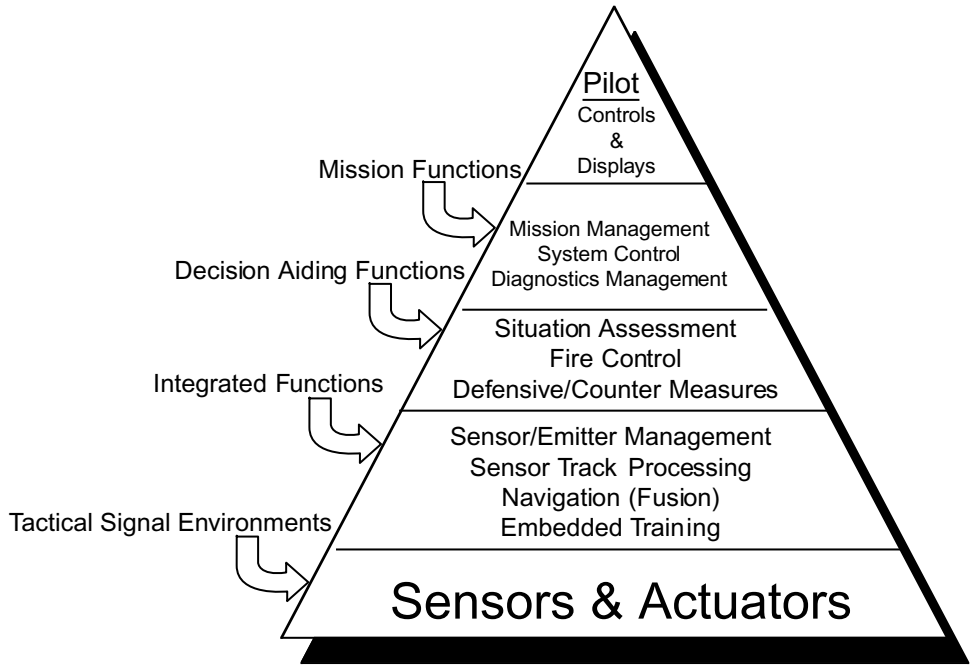

FIGURE 32.2 Avionics functional hierarchy.

First, *situation assessment* is done on the target track relative to the pilot's own ship threat and targeting environment. Consistent and timely information is continuously updated on the overall own ship situation, allowing the pilot to make key decisions to engage or avoid targets of interest. Second, *fire control assessment* calculates missile launch the envelopes against designated targets and controls launch and post-launch weapon support throughout the engagement. Finally, *continuous assessments* are made of the F-22's defensive tactical situation to assist the pilot in managing defensive countermeasures. These decision-aiding functions provide the pilot consistent and reliable tactical information to support war fighting decisions without the need to control individual sensors or correlate target track information in the heat of battle.

At the top level of the mission software hierarchy, mission functions control all avionics hardware and software and status the health of the IAS. These functions handle mission planning and system reconfiguration should hardware failures occur. Being at the top level of control for the IAS, the mission functions are the primary interface between the IAS and the pilot, who interacts with the IAS via *Controls and Displays*.

32.3 Integrated Avionics Architecture

The F-22 avionics architecture is characterized as a common, modular, highly integrated system. These characteristics result in increased performance, reliability, availability, and affordability. It is the first fully integrated avionics system in U.S. military aircraft, supplanting the *federated* architectures of the past. The F-22 does not employ traditional, single-function "black boxes" to perform basic avionics functions such as navigation, communications, threat warning, and fire control. Instead, these functions are implemented with common, programmable modules which are software-configured to process many different functions. This architecture not only allows increased mission effectiveness, but also allows significant flexibility in basic avionics design through: robust, fault-tolerant reconfiguration capabilities, higher reliability, easier supportability, higher availability, lower weight, extended growth capability, and lower acquisition and life cycle cost.

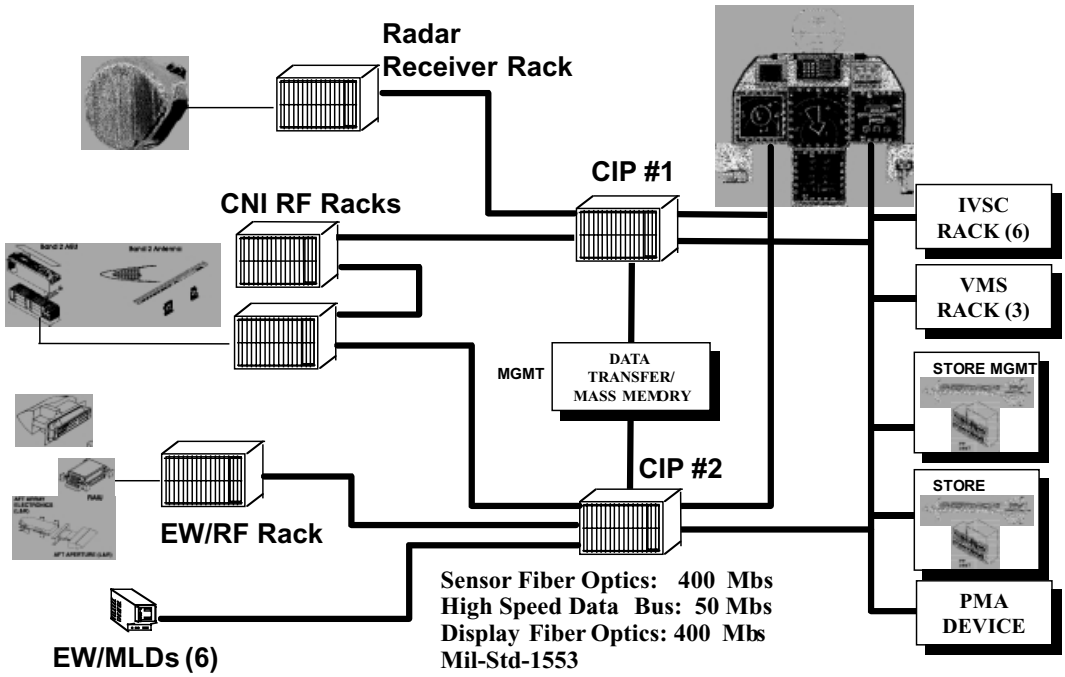

FIGURE 32.3 Avionics system architecture.

The IAS's system design features an interconnected set of high-speed, modular subsystems which use Standard Electronics Module Size E (SEM-E) modules. The core processing architecture is a distributed, parallel processing design that employs common, general purpose digital processor modules to perform all avionics functions. A common operating system is distributed on all core processing SEM-E modules to provide maximum flexibility and to support additional modules for new applications or for technology insertion.

IAS software, written mostly in Ada, is being built and integrated under a multiblock process to reduce development and integration risk. Each software block provides an increase in F-22 functional capability. Block 0 provides basic flight systems for initial flight qualification testing. Block 1 provides single-sensor threads of the IAS system. Block 2 provides multiple-sensor threads. Finally, Block 3 provides full F-22 functionality.

The IAS is partitioned into several interactive systems of antennas, sensors, processors, pilot interfaces, and high-speed interconnects (see Figure 32.3). The primary subsystems are Core Processing (consisting of two Common Integrated Processors, or CIPs), Electronic Warfare (EW), Radar, Communications/Navigation/Identification (CNI), Inertial Reference System (IRS), Stores Management System (SMS), and Controls and Displays (C&D).

By using low observable (LO) antennas and arrays, the sensors receive, measure, and extract both radio frequency (RF) and non-RF signals. Raw data are preprocessed, digitized, and routed to the CIPs via 400 Mbps fiber optic buses. Using digital and signal processor modules, the CIPs process raw data into sensor-level track reports which in turn are processed by sensor-track fusion algorithms residing on other digital and signal processor modules. Sensor-level reports are then combined into a single integrated track file and sent to the cockpit displays via fiber optic lines. The two CIPs are connected to one another via a 50 Mbps fiber optic High-Speed Data Bus (HSDB). Finally, the avionics architecture also features Mil-Std-1553 buses to interconnect to other aircraft systems.

32.3.1 Common Integrated Processor (CIP)

The Common Integrated Processor (CIP), developed by Raytheon Systems Company, provides the memory, I/O, data, and signal processing capability required for the IAS. It has an open, expandable architecture supporting radar, EW, CNI, mission software and Controls, and Displays processing requirements. The F-22 core processing system uses two installed CIPs (with growth space for a third). Each CIP contains 66 SEM-E slots in two rows. Due to the wide utilization of common modules, only 13 unique CIP module types are utilized. To provide for additional growth, each CIP is about two-thirds populated.

32.3.1.1 CIP LRM Types

The *Dual Data Processing Element* (DDPE) is the backbone of the CIP's digital processing capability. Each DDPE has two independent, 32-bit, 25-MHz Intel 80960 (i960®) microprocessors on each side of a SEM-E module. Each side of the DDPE operates as a general purpose computer executing Ada code. The DDPE module is Liquid Flow-Through (LFT) cooled, weighs 1.2 lb and is connected to the CIP backplane by a standard connector which uses 332 electrical pins and 4 fiber optic and two coolant connections. The IAS employs13 DDPEs to support radar, EW, CNI, and MS/W functions. Currently, product improvement programs plan to replace the Intel i960® with a state-of-art processor in 2005.

The *Dual Signal Processing Element* (DSPE) is a generic signal processor that executes mathematically intensive functions such as the state matrix multiplications used in Kalman filter propagation and Fast Fourier Transform (FFT) algorithms used in radar signal processing. Each DSPE uses two independent pipelines to perform high bandwidth signal processing. Each individual SPE can execute a fixed point instruction within one 25 MHz clock cycle and can operate at up to 18 operations per instruction. The DSPE consumes nearly 80 W of power, resides on a Liquid Flow-Through (LFT) cooled SEM-E module, and is connected to the CIP backplane by a standard connector (332 electrical pins and 4 fiber optic and two coolant connections). The IAS employs 9 DSPEs to support radar, EW, and MS/W functions.

The *DPE/Mil-Std-1553 I/O Port* (DPE/1553) features a Data Processing Element (DPE) on side A and a Mil-Std-1553 I/O interface port on side B.

The *Global Bulk Memory* (GBM) is a memory complex available to modules residing on the CIP backplane. Each GBM features 12 Mbytes of available bulk memory, consumes about 60 W of power, resides on a Liquid Flow-Through Cooled (LFT) SEM-E module, and is connected to the CIP backplane by a standard 360-pin connector.

The *Gateway* module (GWY) provides a bi-directional communications path between Parallel Interface (PI) bus segments within a CIP. The GWY module also provides communications between two CIPs via the fiber-optic HSDB.

The *Low Latency Signal Processor* (LLSP) uses a Texas Instruments SMJ320C31 (C-31) processor to provide the interface between the CNI front end and the CIP backplane via a fiber optic line. It performs low latency signal processing for the CNI system.

The *Graphics Processor/Video Interface* (GPVI) features a fiberoptic interface to the cockpit Multi-Function Displays (MFDs). One side of the GPVI module is a standard DPE, the other side performs graphics processing and I/O, generating up to 30 frames per second and supporting up to two MFD displays simultaneously.

The *Non-RF Signal Processor* (NRSP) is an Infra-Red (IR) signal processor that includes a pipeline processing structure optimized to perform IR impulse-response high-pass filtering, two-dimensional windowing for spatial filtering, data normalization, and thresholding for IR sensors. One NRSP can support up to three Missile Launch Detectors (MLDs).

The *Data Encryption/Decryption Device* (KOV-5) is an integrated Communications Security (COMSEC) unit housed in a SEM-E module. It can perform any 2 of 17 different COMSEC, data encryption, data decryption, cryptographic functions. The KOV-5 supports encryption/decryption functions of voice, text, data, and communications links. The encryption/decryption engine is National Security Agency (NSA) certified. The IAS employs 5 KOV-5 modules to support various crypto functions.

Voltage Regulator modules (VR) receive +270 VDC aircraft power and output +5 VDC and −5.2 VDC to the CIP backplane.

The *User Console Interface* (UCIF) is a two-sided LRM featuring a DPE on side A and UCIF hardware on side B. The UCIF is a nonproduction module which supports instrumentation and access to the CIP I/O backplanes during integration and test activities.

The *Fiber Optic Transmit/Receive Network Interface* module (FNIU) provides low latency, high bandwidth communications between a CIP processing cluster and the sensors. The FNIU supports bi-directional communications to the Parallel Interface bus or directly into the GBMs at the rate of 400 Mbps to the GBMs.

32.3.1.2 CIP Buses

The CIPs interconnecting communications paths consist of both internal and external buses. These communications paths are depicted in Figure 32.4.

The *Parallel Interconnect* (PI) Bus is a 32-bit, error-correcting, parallel, digital data bus that facilitates data and control exchange between modules within the CIP at a peak rate of 50 Mbytes per second. Each CIP contains three PI bus segments connected in a "triangle" by three Gateway modules. Each segment supports 22 modules. To optimize communications, subsystem processing (such as radar or EW) is usually clustered into modules within the same PI bus segment.

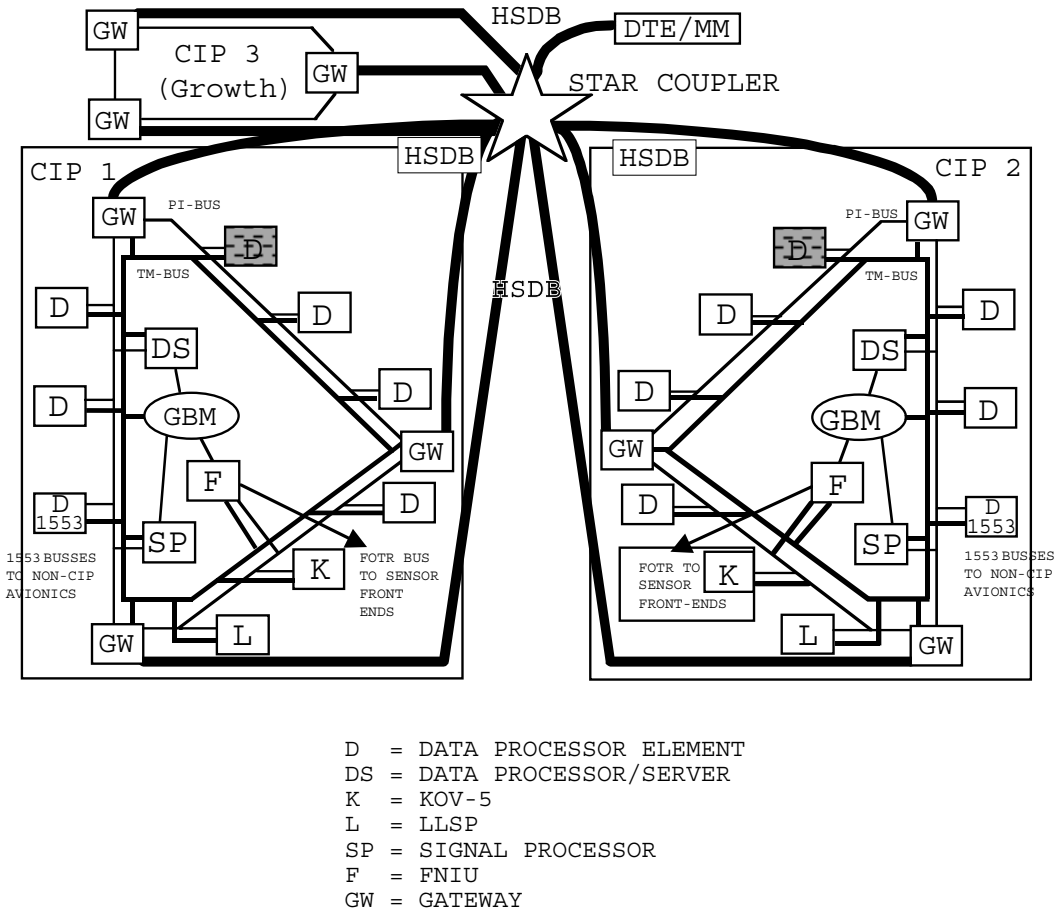

FIGURE 32.4 Simplified CIP structure.

The *Test and Maintenance* (TM) Bus, like the PI bus, contains three segments connected by the Gateway modules. The TM bus is a 6.25 MHz bus primarily used for diagnostic monitoring of each module's health without interfering with either the PI bus or the internal processing within each module. The TM bus also supports fault reporting, isolation, and system reconfiguration. Via the TM bus, spare modules, typically DDPEs, can be commanded to reconfigure to maintain functionality lost due to a failed module.

The *High-Speed Data Bus* (HSDB) is a fiberoptic bus which provides 50 Mbps data transfer rate between the CIPs and the Data Transfer Cartridge or Mass Memory unit.

The *Fiber Optic Transmit-Receive* (FOTR) Bus supports low latency, high bandwidth (400 Mbps) data communications between the CIP and the sensors.

The *Mil-Std 1553* Bus provides I/O communications to standard interfaces such as weapons and aircraft flight control systems.

32.3.1.3 CIP Software

The CIP software has a layered architecture which provides a common set of utilities for the CIP application software and handles data transfer integrity and security. It consists of two principle software packages, the *Avionics Operating System* (AOS) and the *Avionics System Manager* (ASM). The layered architecture with AOS and ASM as an intermediary between the hardware and applications is shown in Figure 32.5.

The AOS provides operating system services to embedded avionics applications running on the CIP. The AOS resides and executes on each DPE-based module. It supports a multilevel secure execution environment in which multiple application programs may run and process concurrently at different security levels. This is enforced by the AOS Privilege Control Tables (PCTs) which require that data at a given security level not be processed by a program at a lower security level. Communications between application programs is restricted to those that are allowed by the PCT. The AOS provides four basic capabilities within the CIP: control of Ada application programs, control of the I/O interfaces to the DPE modules, debug capability, and PCT security access authorization.

The Avionics System Manager (ASM) is the central resource manager for the CIP, featuring three basic services: (1) system control, (2) module management, and (3) file services. It assigns global resources, such as memory and processing elements, to the application programs. ASM is also responsible for maintaining CIP health status, performing reconfiguration around failed modules, providing file management functions between applications and the DTC/MM, providing GBM file allocation services, and coordinating startup and shutdown of CIP functions.

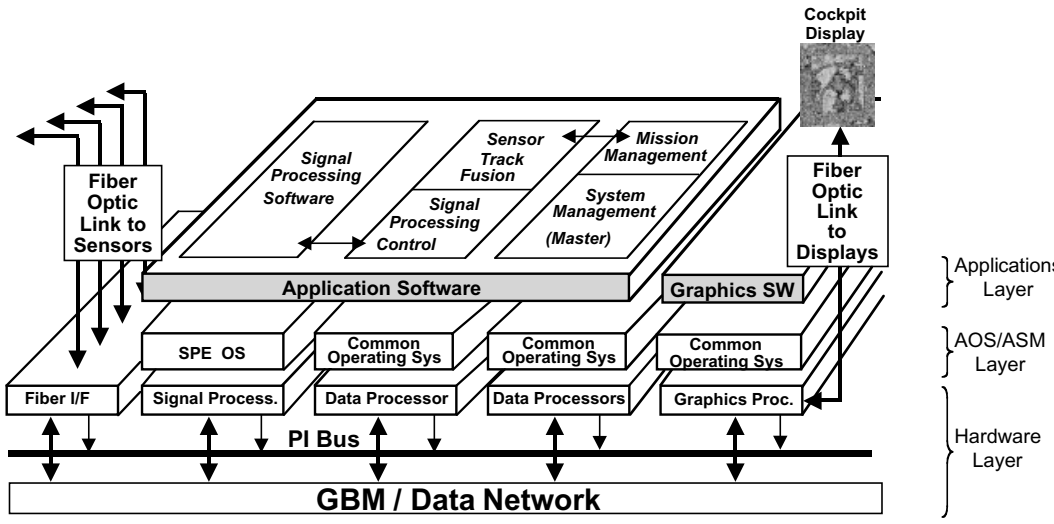

FIGURE 32.5 CIP processing architecture.

32.3.1.4 CIP Signal Flow

The sensor front-ends preprocess RF and non-RF data, converting raw sensor data into blocks of digitized data that are sent, via 400 Mbps FOTR lines, to the FNIUs. The FNIU modules route the raw digitized data to the GBM modules in real time for temporary buffering and storage. The data are then extracted over the Data Networks (DN) by either the DPE or the SPE modules for further processing and refinement. To reduce PI bus overloading, the GBM also supports intermediate buffering of data between the processors or between processing tasks on a processor. Processed data are then sent out on the PI bus to be further processed by other higher-order functions on other DPEs and SPEs. Once these DPEs and SPEs complete the higher-order functional tasks, the data are again sent on the PI bus to the GPVI modules, transferred to graphic format, and sent via FOTR lines to the cockpit displays.

This signal and data flow approach reduces bus loading and potential throughput problems. Sensor data are sent nearly real-time via FOTRs to GBMs and on through the "backdoors" via the DN bus to the processors. Only after the processors have completed their operational tasks on sensor data is the PI bus involved.

32.3.2 APG-77 Radar

The F-22's APG-77 radar is an advanced multimode, multitarget interleaved search/track, all-weather, fire control radar. Developed by Northrop Grumman, it incorporates the following design features: Active Electronically Scanned Array (AESA), low observability (LO), electronic counter-countermeasures (ECCM), and low probability of intercept (LPI). These features give the F-22 radar a major leap in combat capability. The main array, mounted in the nose radome, is composed of hundreds of Transmit/Receive (T/R) modules. Beam switching is performed by controlling each T/R module's phase characteristics, thus accomplishing a summed beam pattern of all T/R modules. These T/R modules are designed to operate for over 16,000 hours failure-free. The T/R module application features an extremely fault-tolerant design, where the system can lose numerous T/R modules before minimum required performance is affected. The system can continue to effectively operate with loss of even more T/R modules, however at reduced transmit power levels.

32.3.3 Communication, Navigation, Identification (CNI)

The F-22 CNI subsystem performs standard military communications, navigation, and identification functions. Developed by Lockheed-Martin Tactical Aircraft Systems (LMTAS) and TRW Military Electronics and Avionics Division, its primary functions consist of UHF/VHF secure and clear voice, Have Quick IIA, GPS, TACAN, ILS, MK XII Identification-Friend-or-Foe (IFF), JTIDS receive, and the Intra-Flight Data Link (IFDL). Like the CIP, the CNI architecture is also highly integrated and uses common SEM-E modules with diverse CNI functions sharing common hardware components. This integrated approach requires time-sharing and multiplexing of assets or system reconfiguration between mission phases (landing vs. engagement operations, for example).

The CNI subsystem is comprised of six major components:

1. Low observable apertures and arrays;
2. External Aperture Electronics (EAE) units (located near the arrays for low noise amplification),
3. RF filtering and switching; the Antenna Interface Unit (AIU) (to interface all RF lines to/from the RF/Preprocessor racks);
4. RF/Preprocessor Integrated Avionics Racks (IARs) which house SEM-E modules for RF transmission, reception, and processing;
5. Interphone/Intercom subsystem for voice communication and synthesis; and
6. CNI digital processing LLSP and KOV-5 LRMs resident on the CIP.

The RF/Preprocessor IARs consist of a pair of three-bay, SEM-E modular, liquid-cooled racks and the LRMs which perform CNI RF processing. The two IARs were originally fully redundant and identical, but to save weight each IAR is now more specialized. However, aircraft mission-critical functions such

as UHF/VHF communications, ILS, TACAN navigation, or MK XII IFF transpond can be supported from either rack.

The CNI SEM-E modules which comprise the CNI IAR racks are as follows:

1. Eight L-Band tunable receivers with selectable IF bandwidths to support TACAN, MK-XII transponder, Mode S ATC, IFDL, and JTIDS receive.
2. Two 5-channel tunable L-Band receivers with common local oscillators used to support direction finding.
3. One L-Band transponder Carrier Generator/Power Amplifier (CG/PA) used to support low duty cycle pulse modulation of RF transmit power for MK XII IFF transponder and TACAN functions.
4. One Interrogator CG/PA used to provide low duty cycle RF pulse modulation for MK XII interrogate. This CG/PA is used as a backup for MK XII transpond and TACAN in the event of an L-Band Transpond CG/PA failure.
5. Four UHF/VHF single-channel tunable receivers which support U/VHF voice communications, ILS, and growth satellite communications.
6. Two UHF/VHF CG/PAs for supporting U/VHF transmit.
7. One GPS Receiver Processor to provide a complete decoded GPS navigation solution.
8. Two RF/FE controller LRMs which support all RF asset control, multiplexing, timing references, and reconfiguration.
9. Four Pulse Narrowband Processor (PNP) LRMs used to support L-Band programmable pulsed signal decoding such as TACAN, MK XII IFF transponder, and interrogate, and Mode SATC. The PNP LRM also supports A/D conversion of the U/VHF communications and ILS navigation.
10. One Pulse Environment AOA Processor (PEAP) LRM to convert measured pulse phase and magnitude data into a calculated Angle of Arrival (AOA) via algorithms which use real-time calibration data and prestored array characteristics.
11. Two CNI Bus Coupler LRMs to provide a FOTR bus interface to the FNIU module within the CIP.
12. One IFDL Mod/Synth LRM to provide the waveform generation, signal modulation and demodulation, and relative navigation processing for the F-22-to-F-22 Intra-Flight Data Link system.

Other SEM-E modules are the Air-Combat Maneuvering Instrumentation (ACMI) transceiver which provides ACMI signal modulation and demodulation; the Ovenized crystal oscillator LRM; a 5-volt backup battery LRM used to maintain system crypto keying and clocks with main power off; and various RF and digital power supply LRMs which provide up to seven different voltages required by the CNI system components.

32.3.4 Electronic Warfare (EW)

The EW subsystem provides Radar Warning (RW), Missile Launch Detection (MLD), and chaff and flare countermeasures. RW was developed jointly by Lockheed Martin Missiles and Fire Control, Lockheed Sanders, and LMTAS. It provides airborne and ground-based radar emitter detection, tracking, identification, and location to the mission software system for integrated target tracking. The Missile Launch Detector also provides a passive IR capability to detect, declare, track, and report missile launches to mission software. The defensive countermeasures function is responsible for timing and deploying chaff and flares. Deployment of countermeasures is programmable for fully automatic, semiautomatic, or manual.

The EW architecture, like the CIP and CNI, is an integrated architecture using common SEM-E modules. The EW subsystem employs resource sharing of common hardware components to perform the simultaneous search, detection, RF and non-RF measurement, signal analysis, direction finding, identification, and tracking of RF and non-RF signals. This integrated approach requires time and resource sharing of these common modules.

The EW subsystem is comprised of seven major components:

1. Low observable apertures and arrays;
2. Array Electronics (AEs) units near the arrays for low noise amplification, RF filtering, and switching;

3. Remote Antenna Interface Unit (RAIU) to interface all RF lines to/from the EW RF racks;
4. EW RF Integrated Avionics Racks (IARs) which house SEM-E modules for RF, reception, and processing;
5. Six Missile Launch Detector sensors;
6. The countermeasures controller and dispenser units to dispense MJU-7 and -10 standard flares, MJU-39 and -40 flares developed specifically for the F-22, and RR-170 and -180 chaff bundles, and
7. The CIP based DDPE, DSPE, NRSP, and GBM LRMs.

The EW RF IAR consists of a SEM-E modular liquid-cooled rack and the LRMs which perform the EW RF reception and processing. The EW SEM-E modules which comprise the EW RF IAR rack are as follows:

1. Six Narrow-Band Receiver (NBR) LRMs with selectable IF bandwidths to support signal analysis, emitter tracking, and emitter direction finding processing.
2. Six NBR Local Oscillator LRMs to tune the NBRs.
3. Six Pulse Measurement Units to extract RF characteristics from the NBR for signals analysis.
4. Four Wide-Band Receiver (WBR) LRMs to support wideband detection and acquisition of emitters in the environment.
5. Six signal frequency down converter LRMs to convert RF signals into a base frequency band.
6. Nine power supply LRMs to convert 270 V power to +/−9, +/−15 and +/−5 V.
7. One WBR asset controller LRM.
8. One NBR asset controller LRM.
9. Two RF Delay LRMs to support hand-off of signal analysis for direction finding processing.
10. One Reference Oscillator LRM for supplying a common local oscillator to the NBR and down converter LRMs.
11. One CIP Interface (CIPI) module to interface digitized EW information onto the CIP fiber optic FOTR bus.
12. One Data Converter LRM to reformat digitized RF data into pulse descriptor words for CIP processing.
13. Three Measurement Control Processor (MCP) LRMs to support timing and synchronization of receiver assets.
14. One Data Distribution Network (DDN) to provide DF triggers for supporting signal direction finding and angle binning to support pulse de-interleaving.
15. Two Compressive Receiver (CR) LRMs to support high probability of intercept against high priority signals.
16. One Array-RAIU Controller Interface (ARCI) to control RF line switching and filtering in the RAIU.

The EW RF IAR racks perform RF to digital conversion and then send the raw digitized information to the FNIU fiber optic interface module in the CIP for RF sorting, signal characteristic measurement, signal identification, and emitter tracking.

32.3.5 Stores Management System (SMS)

The SMS monitors, controls and statuses countermeasures, launchers, weapon bay doors, and the F-22 armament (AIM-9, AIM-120, gun). It also controls emergency jettison of stores. The SMS consists of two rows of SEM-E modules, two AIM-9 power supplies, a gun control unit, and the SMS Controller.

32.3.6 Inertial Reference System (IRS)

Developed by Litton Guidance and Control, the IRS is an advanced laser ring gyro with a common processor with flight controls. It provides position and rate information to the IAS mission software to support target location calculations.

32.3.7 Controls and Displays (C&DS)

Unlike today's generation of fighters, the F-22's tactical displays are not dedicated to providing sensor-only information such as radar-only displays. Instead, the F-22 has four active-matrix liquid-crystal Head-Down displays (HDD) and a Head-Up display (HUD) to provide highly integrated information concerning the overall tactical situation. The middle HDD, or Tactical Situation Display (TSD), is an 8 × 8 in. color display that provides the pilot with current situational awareness and enhanced navigational information, including location of airborne friendlies and threats, ownship heading, navigational waypoints, etc. The left 6 × 6 in. color HDD, or Attack Display, provides the pilot with the current offensive tactical situation and is tailored for weapons employment including target selection and offensive and defensive missile engagement ranges. The right 6 × 6 in. color HDD, or Defensive Display, provides the pilot with the current defensive tactical situation and is tailored for assessing threat capability against the F-22 and includes location and identification of airborne and ground-based engagement systems, missile engagement ranges, and countermeasures selection. The lower 6 × 6 in. color HDD provides status of aircraft expendables, stores, engine performance, and external doors status.

32.4 Fault Tolerance and Recovery

Another characteristic of F-22 avionics is its robust fault tolerance and fault recovery by means of reconfiguration — a mechanization that restores needed functionality after loss or failure of assets. Reconfiguration is achieved by reallocating and/or reprogramming modular resources. Recovery implies full operational capability or a degraded mode of operation, depending on the number of spare modular assets left to support reconfiguration. "Minor reconfiguration" occurs due to the loss of a module (or several) and "major reconfiguration" occurs due to the loss of an entire rack. Major reconfiguration can be caused by battle damage, loss of an engine and/or generator, or overheating due to loss of cooling. Major reconfiguration is the ability to reprogram and reconfigure a fully functional SEM-E rack to support emergency backup functions such as UHF voice communications, TACAN navigation, instrument landing system navigation, and MK XII identification for safe return to base or to complete a critical part of the mission. Minor reconfiguration is accomplished by reprogramming modules to perform functions lost by the failure of an identical common module. Minor reconfiguration is driven by a function prioritization table. Once all spare modules of a common type have been used, the lowest-priority function is dropped to support higher-priority functions. The common modular approach and reconfiguration flexibility results in outstanding mission availability and graceful degradation.

32.5 Summary

The F-22 program is completing the manufacture of its nine EMD aircraft and moving into production; 339 aircraft are scheduled to be produced. The F-22 IAS is developed in three major functional blocks. IAS flight testing will be complete in mid-2002. Flight testing on the first block is to begin on air vehicle number 4, which is the IAS-equipped aircraft, in mid-2000. F-22 Initial Operational Capability is scheduled for December 2005.

The IAS places robust, first-of-its-kind, fully integrated tactical war fighting capabilities into the hands of the pilot. The key avionics contribution to the F-22's unprecedented combat effectiveness is its ability to perform fusion of multisensor information to provide the pilot integrated target detection, identification, tracking, and threat warning information on his displays, significantly reducing the pilot workload during battle conditions. The common, modular, and open architecture allows the needed flexibility to handle growth in the face of ever-changing threat and advancements in avionics technology. The integrated IAS architecture and its superior functional capabilities in conjunction with the advanced F-22 capabilities in stealth, maneuverability, super cruise, and advanced armament will ensure F-22 air superiority and mission effectiveness well into the 21st century.